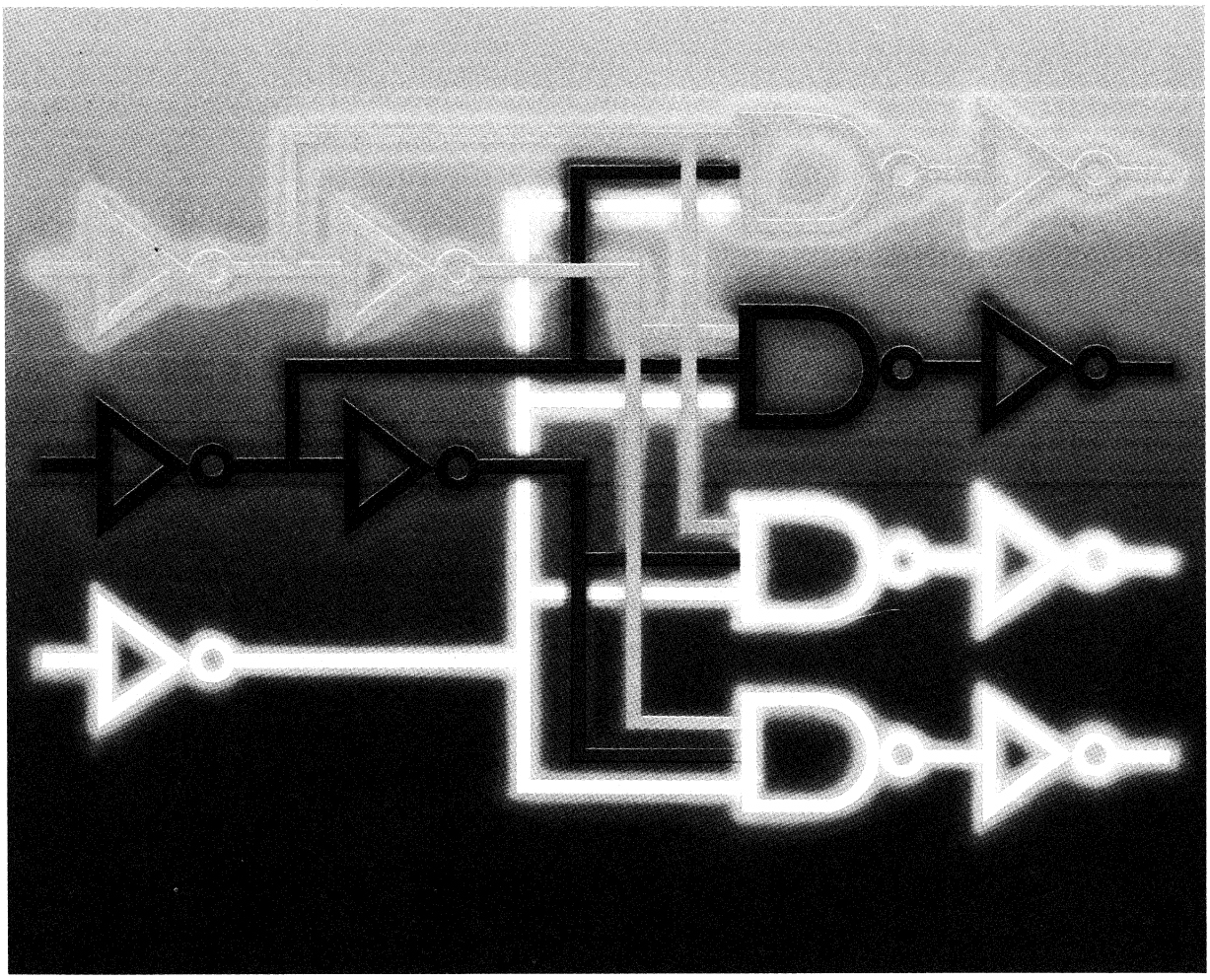
CMOS Commodity Logic ICs



Phase-locked loop circuits: 74HC/HCT4046A & 74HC/HCT7046A

HCMOS designer's guide - advance information

Philips Components

PHILIPS

Note:
The full type number of the HCMOS products mentioned in this publication is 74HC/HCTxxxx. Both the HC and HCT versions are specified for a temperature range of –40 °C to +125 °C. For brevity, where it isn't required to distinguish between HC and HCT versions, the prefixes 74HC and 74HCT are omitted.

Phase-locked loop circuits: 74HC/HCT4046A & 74HC/HCT7046A

BY R. VOLGERS

HCMOS designer's guide - advance information

CONTENTS

The development of single-chip PLLs has brought about an enormous growth in the use of phase-locked loop (PLL) techniques throughout electronic engineering. Formerly, uneconomic or impractical in many applications, PLL techniques are now in widespread use, bringing excellent noise immunity and tracking ability to ever more designs. In the field of communication, the applications for PLLs include frequency synthesizers, data modems, clock regeneration and FM and AM demodulators, to name but a few examples. In other fields too, PLLs are widely used, for example, in motor speed-control systems, tracking voltmeters and spectrum analyzers.

The aim of this publication is to assist those designing with Philips high-speed CMOS (HCMOS) integrated PLL circuits. With this in mind, there is a design program[1] which can be used to put many of the principles described here into practice. The program which runs on an IBM PC, or compatible, enables PLLs to be designed and optimized fast. The effect of altering loop parameters can be readily observed. For many, the design program alone will suffice; for those requiring more insight into the theory behind the workings of the program, the chapter 'PLL Analysis' is included in this publication.

The PLL circuits described (the 74HC/HCT4046A and 74HC/HCT7046A) are high-speed silicon-gate CMOS ICs and are specified in compliance with JEDEC standard No. 7. Both circuits are available in a 16-pin DIL or a 16-pin SO package. The 4046A is pin-compatible with the '4046' of Philips' HE4000B series (except for pin 15, the ZENER input of the HE4000B circuit, which is now used as the output of an additional phase comparator); the 7046A is a new IC.

PLL BASICS

A PLL is basically a feedback system which synchronizes an oscillator in phase and frequency to an incoming signal. A PLL has three main parts: a phase comparator, a low-pass filter and a voltage controlled oscillator (VCO), see Fig.1. The phase comparator measures the phase difference between the input and output signals and produces an error signal proportional to the measured phase difference. If the low-pass filter is disregarded for the moment, the error signal will drive the VCO, changing its frequency so as to minimize the phase difference between the input and output signals.

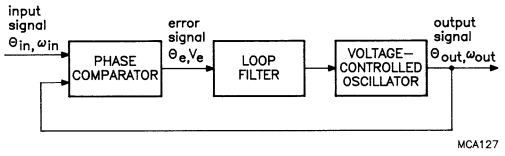


Fig.1 Basic phase-locked loop. V_e is the average error voltage.

Ultimately, the frequency of the output signal will be identical to that of the input signal and will follow every change of the latter. However, if the error signal is low-pass filtered, the VCO will not react to high-frequency changes or noise in the input signal and will run at only the average frequency of the input signal. This electronic flywheel characteristic of a PLL is the one that is most used. To enable a PLL to acquire lock in the first place, it should of course be designed so that the difference between the input and output frequencies is not so large that, after filtering, there is no control signal for the VCO.

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[1]available from Philips Components, ordering code 9398 650 00011.

TYPES OF PLL

There are analog PLLs and digital PLLs, the main difference being the phase comparator used. In an analog PLL, the phase comparator is often a four-quadrant multiplier or mixer using high-performance analog amplifiers to produce a pure sinusoidal output from a sinusoidal input. This type of linear PLL is often used to detect and retrieve very weak signals from a noisy communication channel.

The 4046A and the 7046A PLL circuits have digital phase comparators, chosen because they can be used in virtually every PLL application. A self-biasing input stage enables them to operate with AC input signals as low as 20 mV (peak-to-peak) at V_{CC} = 4.5 V, as well as with signals between the HCMOS family input logic levels. Although these circuits have digital phase comparators, the VCO is controlled by an analog signal – the average output voltage of the phase comparator. A wholly-digital HCMOS PLL circuit is available – the HC/HCT297. In this circuit, the VCO is replaced by a 'pulse swallower'. Further details are available in the publication "All-digital PLLs using the 74HC/HCT297", ordering code 9398 065 90011, Philips Components.

PLL TERMINOLOGY

There is a multiplicity of terminology in common use for PLLs. Therefore, it is useful to list the terminology used throughout this publication before the description of the 4046A and 7046A. Only the main PLL terms are listed here; a complete glossary of symbols and terms appears in Appendix D.

Hold range: $\pm\Delta\omega_H$ (see Fig.2)

The range of frequencies over which a loop will remain locked. A loop is considered to be out of lock when the maximum permissible phase error is exceeded.

For the 4046A and 7046A HCMOS circuits, the hold range is only valid when phase comparator PC1, or PC3, and a passive low-pass filter are used, see 'Phase comparators', page 12. When comparator PC2 or an active filter, or both, are used, the hold range is equal to half the output frequency range of the VCO.

Pull-in range: $\pm\Delta\omega_{PI}$

The frequency range over which the PLL can acquire lock. This range which is usually less than the hold range is proportional to the natural frequency of the loop (ω_n). The time to acquire lock is called the pull-in time (T_p).

When phase comparator PC2 is used, the pull-in range is equal to the VCO output frequency range, because PC2 is both phase-sensitive and frequency-sensitive.

Pull-out range: $\pm\Delta\omega_{PO}$

The frequency step at the input, referenced to the VCO centre frequency (ω_0), which causes a locked loop to lose lock.

Since the pull-out range is normally within the pull-in range, the loop will reacquire lock (in the pull-in time).

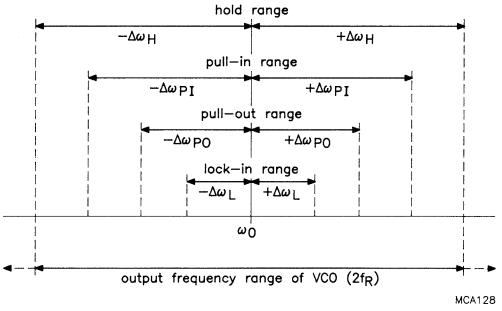


Fig.2 Operating areas of a PLL.

Lock-in range: $\pm\Delta\omega_L$

The frequency range over which the loop can acquire lock without cycle slip.

The time to acquire lock within the lock-in range is called the lock-in time or settling time (T_S). T_S is inversely proportional to the natural frequency of the loop (ω_n). Note that the term settling time is also used in frequency synthesizer applications, where it is the time for the loop's output to settle to within 5% of the applied step, after switching between two channels. This settling time is identified by the symbol $T_{S(5\%)}$.

Centre frequency (free-running frequency): ω_0

This is the output frequency of the VCO when the VCO input control voltage is half of the supply voltage. At this frequency, the VCO is at the centre of all its operating ranges.

Natural frequency: ω_n

The frequency at which the loop would oscillate if it was not damped (that is, if the damping factor $\zeta = 0$). In the Bode plot of the (underdamped) closed second-order loop, the natural frequency is that frequency which gives the largest positive deviation from the DC gain.

Components of the input signal higher than the natural frequency will be damped by an amount depending on the damping factor.

Phase comparator conversion gain: K_d

The conversion constant relating the phase comparator's average output voltage to the phase difference between the signal input and the VCO output signal. K_d has units of volts per radian.

VCO conversion gain: K_o

The conversion gain constant relating the linear frequency range of the VCO ($2f_R$) to the VCO control voltage range. K_o has units of radians per second per volt.

VCO output frequency range: $2f_R$

Although not a system parameter, the VCO frequency range is included here for completeness. It is the maximum output frequency range of the VCO in a particular application.

The 74HC/HCT4046A and 74HC/HCT7046A are very similar. Each circuit has a linear VCO and two phase comparators (PC1: EX-OR, and PC2: edge-triggered) with a common comparator input amplifier and a common signal input amplifier. The 4046A has a third phase comparator (PC3: edge-triggered), while the 7046A has improved lock-detection circuitry. As can be seen in Fig.3, only a low-pass filter and a few external components are needed to form a complete PLL.

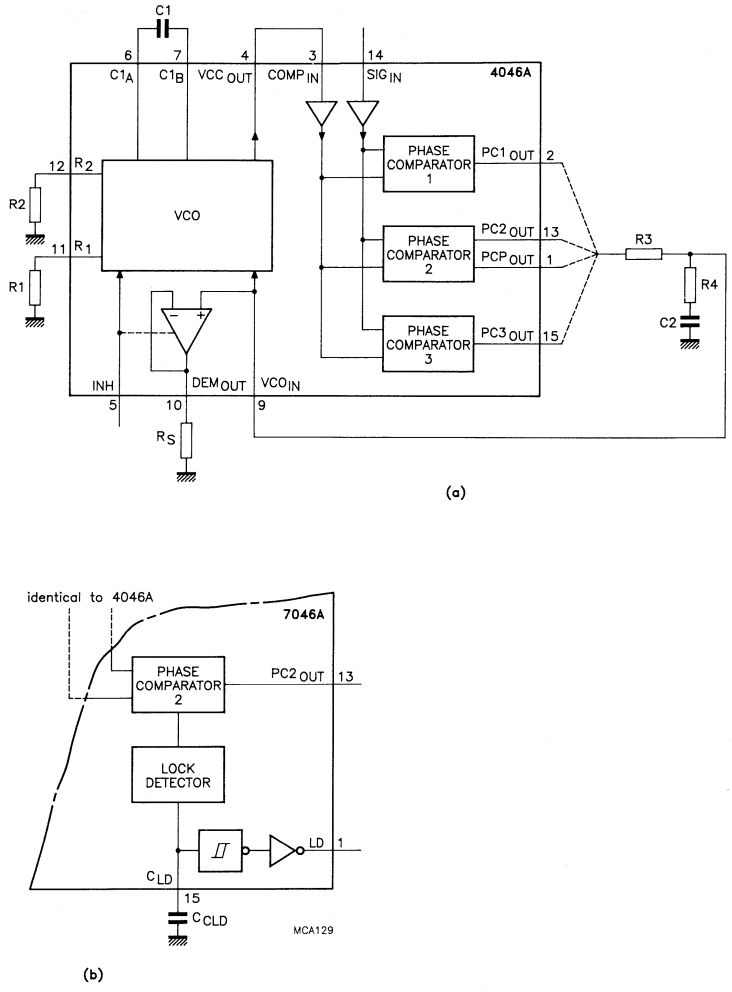


Fig.3 Pinning and functional diagram of (a) the 74HC/HCT4046A and (b) the 74HC/HCT7046A.

Voltage-controlled oscillator

The VCO requires one external capacitor, C1, and one or two external resistors, R1 and R2, to complete (Fig.3). R1 and C1 determine the centre frequency (f_0) and the operating range ($2f_R$) of the VCO (see Figs 4 and 5). R2 enables the VCO to have a frequency offset (f_{off}) if required; the offset depending on R2 and C1 (see Fig.6). The linearity of the VCO is excellent, owing to the use of linear op-amp techniques. An extremely high input resistance (pin 9; VCO_{IN}) enables a wide variety of loop filters to be used.

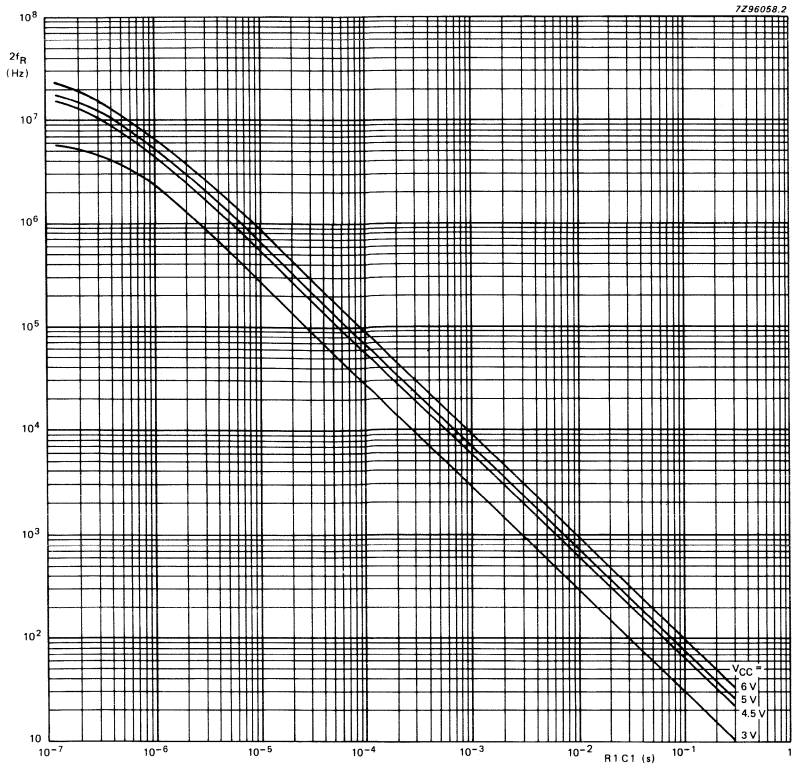


Fig.4 Typical output frequency range of the VCO ($2f_R$) as a function of R1C1. The control voltage ($V_{VCO\ IN}$) range is 1.1 V to V_{CC}–1.1 V; R2 = ∞.

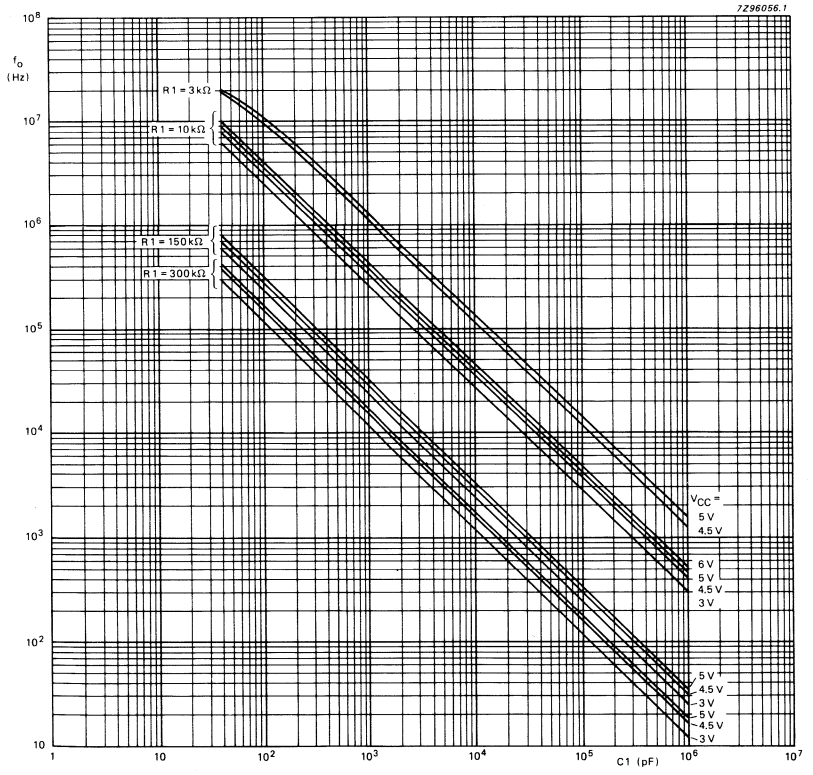


Fig.5 Typical VCO centre frequency (f_0) as a function of C1. R2 = ∞; $V_{VCO\ IN}$ = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C. For optimum VCO performance, C1 should be as small as possible but larger than 100 pF. The curves can be interpolated for other values of R1, because a constant R1C1 product produces almost the same VCO output frequency.

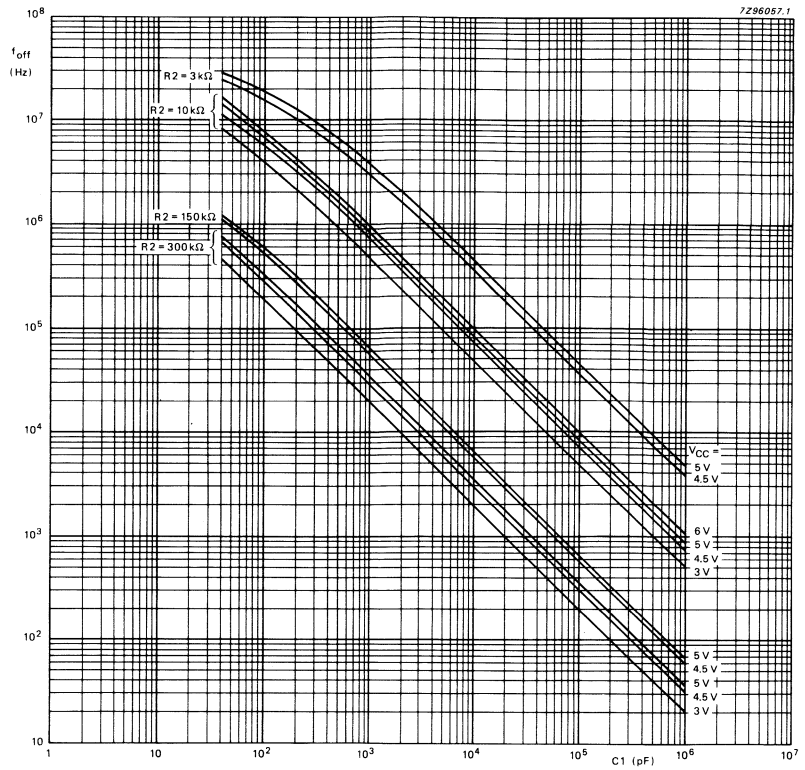


Fig.6 Typical frequency offset (f_{off}) as a function of C1. R1 = ∞; $V_{VCO\ IN}$ = 0.5V_{CC}; INH = GND; T_{amb} = 25 °C. $f_{off} = f_0 - 1.6f_R$.
For optimum VCO performance, C1 should be as small as possible but larger than 100 pF. The curves can be interpolated for other values of R2, because a constant R2C1 product produces almost the same VCO offset frequency.

Figure 7 is a circuit schematic of the VCO. The current I' is mirrored via transistors N1 and N3, the latter providing the bias current for an emitter-coupled input stage whose non-inverting and inverting inputs are the gates of N4 and N5 respectively.

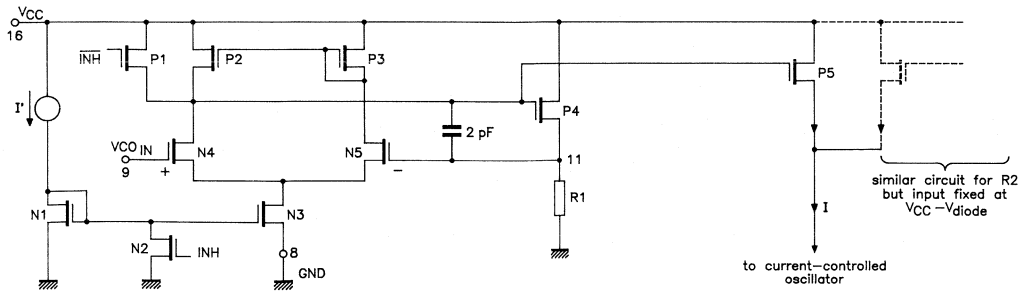
Assume that the gates of N4 and N5 are at the same DC level; both transistors conduct equally and their drains are at the same potential. If the VCO input voltage (on pin 9) is raised, N4 conducts more and its drain voltage falls, increasing the gate-to-source drive of P4 and P5. This in turn raises the potential at pin 11 and hence that on the gate of N5, making the DC levels on the gates of N4 and N5 equal again.

From the above, it can be concluded that:

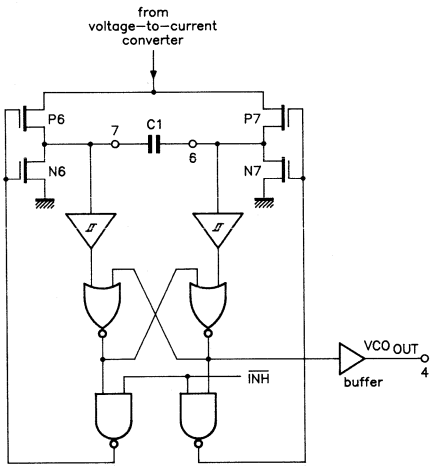
- pin 11 follows the positive input (VCO_{IN}) exactly;
- increasing the VCO input voltage produces a linear increase of the current through R1;
- the current through R1 is mirrored via P5 to the current–controlled oscillator, which generates the charging current for C1 which sets the VCO output frequency.

When one electrode of C1 is charged via P6 (or P7) with the current I, the other is held low by N7 (or N6). When the positive threshold voltage, V_T+, of one of the Schmitt-triggers is reached, P6 (or P7) is turned off and the other terminal of C1 is charged via P7 (or P6), see Fig.8.

An identical circuit in parallel to P5 gives the current contribution of R2, for a frequency offset, only here the non-inverting input of the op-amp is fixed at $V_{CC} - V_{diode}$.



VOLTAGE−TO−CURRENT CONVERTER



CURRENT−CONTROLLED OSCILLATOR MCA131

Fig.7 Schematic of the VCO used in the 74HC/HCT4046A and 74HC/HCT7046A.

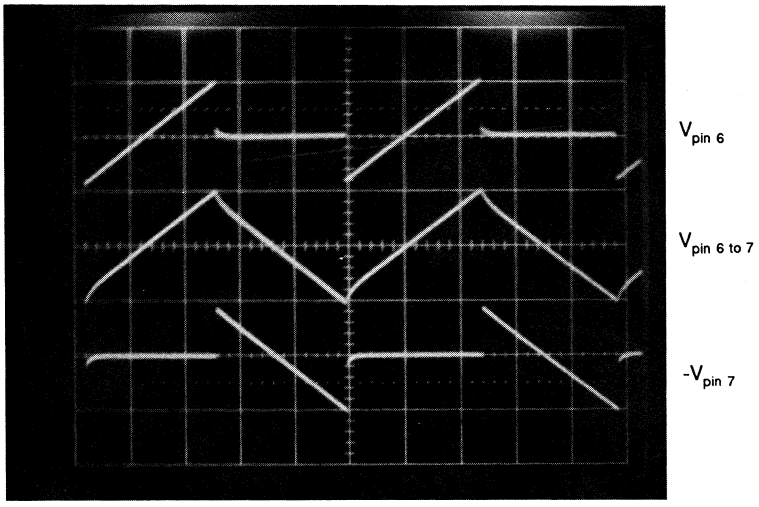


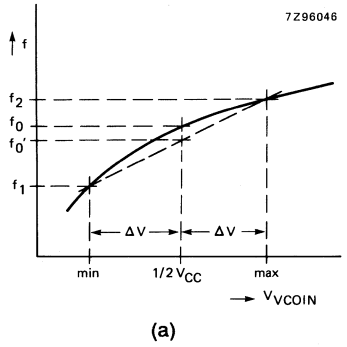
Fig.8 Voltage waveforms at pins 6 and 7 of the VCO (i.e. on both sides of C1).

Linearity

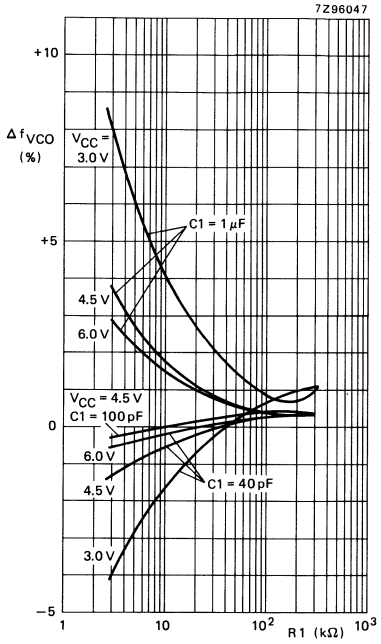
The op-amp technique used in the voltage-to-current converter of the VCO provides excellent linearity (see Fig.9) over the allowed control voltage range of the VCO (1.1 V to V_{CC} – 1.1 V). Control voltages outside this range produce a step in the VCO output frequency, see Fig.10. When the VCO input voltage exceeds V_{CC} – 1.1 V, the VCO oscillates at its highest frequency (>20 MHz). When the VCO input voltage is below 1.1 V, the VCO oscillates at:

- a few Hertz when R2 is not used (see Fig. 10(a)), because the VCO is biased only by internal leakage currents;
- f_{off} (i.e. $f_0 - 1.6f_R$) when R2 is used (see Fig.10(b)).

A properly-designed PLL will never generate signals outside the allowed control voltage range of the VCO, so a control voltage clamp is generally superfluous. A clamp may however be useful in applications where the input signal is outside the VCO frequency operating range for a long time relative to the filter time-constant. A suitable clamp is described in the section 'Application Examples'.

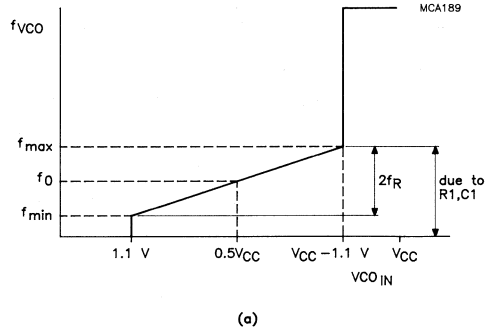


(a)

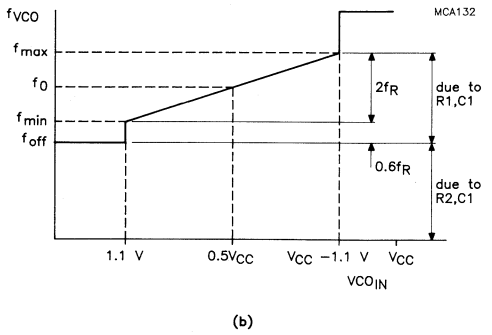


(b)

Fig.9 (a)Definition of VCO frequency linearity: ΔV = 0.5 V over the V_{CC} range: for linearity $f'_0 = (f_1+f_2)/2$, actual linearity = $(f'_0-f_0)/f_0$ x100% (b)Frequency linearity as a function of R1, C1 and V_{CC}. R2 = ∞ and ΔV = 0.5 V.



(a)



(b)

Fig.10 Frequency characteristic of the VCO. (a) without offset; (b) with offset. f_0 = centre frequency; $2f_R$ = VCO linear operating range.

Demodulator output

For demodulation applications, a buffered VCO_{IN} signal is available at pin 10 (DEM_{OUT}) of both the 4046A and the 7046A. An op-amp similar to that used in the VCO buffers the signal, so as not to affect the characteristics of the low-pass filter. The offset voltage is typically only about 20 mV at V_{CC} = 4.5 V.

To bias the output stage correctly, a load resistor (R_S) of between 50 kΩ and 300 kΩ should be connected between pin 10 and ground.

Duty factor

The duty factor of the VCO output signal depends on the symmetry of both branches of the current-controlled oscillator, (i.e. on the symmetry of the Schmitt triggers, NOR and NAND gates and N6/P6 and N7/P7 in Fig.7) and on the on-chip spread of the V_T+ of the Schmitt triggers. Well-balanced transistor sizes and loads limit the deviation from a 50% duty factor to typically ±1% over the full temperature and supply voltage range.

Conversion gain

The conversion gain of the VCO (K_o) depends on the VCO output frequency range ($2f_R$), and varies slightly with supply voltage. Note that the VCO range in Fig.4 is in Hz whereas rad/s should be used when calculating K_o. For example, with a frequency range of 10^4 Hz and V_{CC} = 5 V:

$$K_o = \frac{\text{VCO frequency range}}{\text{VCO input voltage range}} = \frac{2\pi 10^4}{(5 - 2.2)} = 22\,440 \quad \text{rad/s/V.} \qquad (1)$$

Effect of temperature

Figure 11 shows the frequency stability of the VCO as a function of ambient temperature. In a PLL, these frequency deviations of the VCO are, of course, compensated automatically by the loop, only the absolute value of the phase difference between the input signal (pin 14) and the VCO output signal will vary slightly when comparators PC1 and PC3 are used. This is discussed in more detail in the next section.

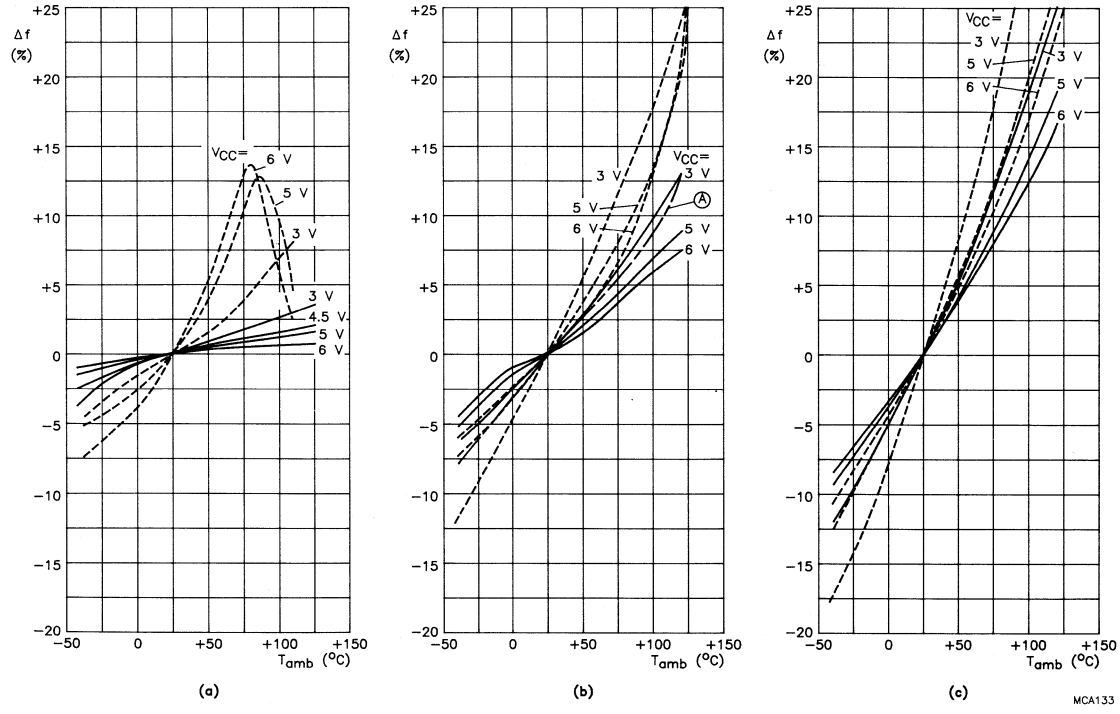


Fig.11 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
—— without offset (R2 = ∞): (a)R1 = 3 kΩ; (b)R1 = 10 kΩ; (c)R1 = 300 kΩ.
- - - with offset (R1 = ∞): (a)R2 = 3 kΩ; (b)R2 = 10 kΩ; (c)R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias curent, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO\ IN}$ = 0.5V_{CC}.

The best stability is at high bias currents together with low values of C1. At high ambient temperatures, the current-to-frequency converter decreases the output frequency, owing to the increased propagation delay of the logic, but not sufficiently to compensate an increasing charge current, resulting in a positive temperature coefficient for the whole VCO as shown in Fig.11.

When there is a frequency offset, the temperature coefficient is larger, because R2 is biased via a diode whose forward voltage is also temperature dependent.

Note that the measurements of frequency stability were taken with R1 and R2 held at a constant 25 °C, which is unlikely in practice. If R1 and R2 are normal metal-film resistors, their positive temperature coefficient will partly compensate the frequency changes due to variations of ambient temperature. In addition, C1 should have a negligible temperature coefficient, e.g. an NP0 capacitor. If both R1 and R2 are used, the total frequency change is not the sum of a pair of curves shown in Fig.11, but is set by the total VCO bias current (curve A).

Phase comparators

Both the 4046A and the 7046A circuits have two different phase comparators:

- PC1: an exclusive-OR circuit
- PC2: an edge-triggered circuit with a 3-state output.

The 4046A has an additional edge-triggered comparator: PC3.

The signal input, SIG_{IN}, and comparator input (usually connected to the VCO output), $COMP_{IN}$, can be directly coupled to the self-biasing amplifiers provided the signal swing is between the standard HCMOS input logic levels. Capacitive coupling is required for smaller AC signals (typically >20 mV peak-to-peak).

Phase comparator 1 (PC1)

This comparator is solely phase-sensitive (i.e. the average output voltage bears no relation to the frequency difference between the input signals). PLLs using it can retain lock with noisy input signals, because the full input signal (not only the rising edges) is used to determine the comparator's average output voltage. The pull-in range depends on the low-pass filter characteristics, and can be made as wide as the hold range. Note that PC1 can lock onto input frequencies close to harmonics of the input frequency.

Function

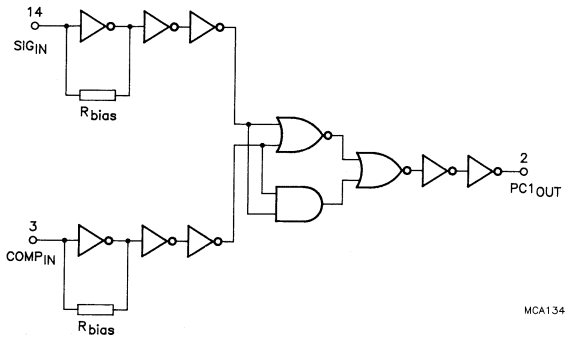


Fig.12 Logic diagram of a PC1 comparator.

When SIG_{IN} and $COMP_{IN}$ have the same polarity, the output of the comparator, $PC1_{OUT}$, is LOW; when they have opposite polarity, the output is forced HIGH. Figure 13 shows the output signal due to a phase difference between SIG_{IN} and $COMP_{IN}$ when the input frequencies are the same.

A phase difference of 90°, see Fig.13(a) (corresponding to an input signal equal to the VCO centre frequency, f_0, or no signal at all) gives an average output of $0.5V_{CC}$ (see Fig.13(d)), causing the VCO to oscillate at f_0.

When the SIG_{IN} input frequency isn't f_0, the VCO input is raised or lowered, depending on the frequency difference, to adjust the VCO output frequency towards the input frequency. The VCO input voltage is altered by changing the duty factor of the output signal of the comparator. If PC1 adjusts the phase difference between SIG_{IN} and $COMP_{IN}$ away from 90°, the duty factor of the comparator's output signal changes accordingly, see Fig.13(b) and (c). Therefore, if the input frequency isn't f_0, the phase difference isn't 90°, but some other value between 0° and 180°.

With the PC1 comparator, only the input frequencies are made equal – the absolute phase difference in a locked loop can be any value between 0° and 180° (unless an active loop filter is used, in which case the phase difference remains at 90°, because the VCO input voltage is generated via an integrator).

For the widest hold range, the signal and comparator input frequencies should have a duty factor of 50%. The effect of a smaller duty factor is illustrated in Fig.14.

In Fig.14(a), the duty factor of $COMP_{IN}$ is only one third that of Fig.13. Now the minimum average output voltage of the comparator is already reached for a minimum phase difference of +60°, while in Fig.14(b) the maximum average voltage is reached with a maximum phase difference of +120°. Outside these values, the average voltage won't change, so the range over which PC1 can adjust has shrunk by the same amount as the duty factor (two-thirds). This means that the lock-in range, hold range, pull-out and pull-in ranges are also lowered by the same amount. And the transfer characteristic (input phase error to average output voltage) has changed from that of Fig.13(d) to that of Fig.14(c).

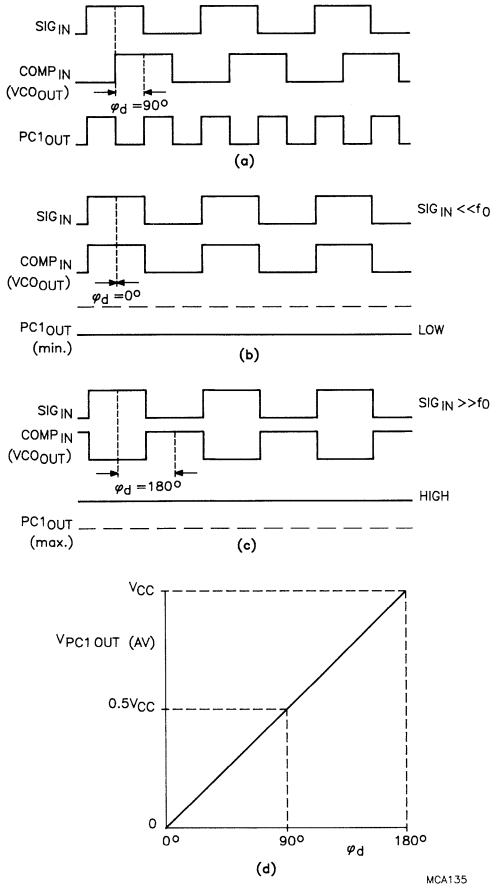


Fig.13 PC1 phase adjustment. Typical waveforms for a PLL with phase differences, ϕ_d, of (a)90°, (b)0°, and (c)180° between SIG_{IN} and $COMP_{IN}$ which are of the same frequency. (d) Average output voltage as a function of input phase difference.

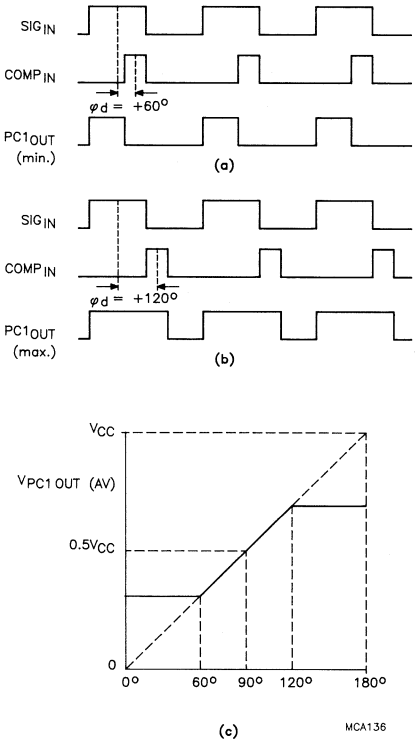


Fig.14 Effect of duty cycle of the SIG_{IN} and $COMP_{IN}$ signals on the output signal of PC1. (a) minimum signal reached at +60° phase difference and (b) maximum signal reached at +120° phase difference by reducing the duty cycle. (c) Average output voltage as a function of input phase difference.

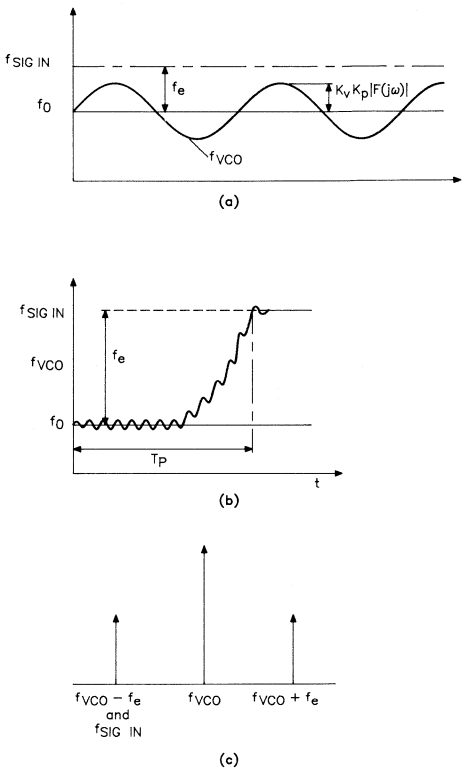


Fig.15 VCO output frequency for comparator PC1 during capture. (a) without a filter; (b) with a filter. (c) frequency spectrum of the frequency modulated VCO output frequency and the input frequency $f_{SIG\ IN}$. f_e is the frequency of the error signal.

Since the SIG_{IN} and $COMP_{IN}$ inputs are fully interchangeable, the average output voltage of the comparator is the same irrespective of whether the SIG_{IN} frequency is higher or lower than $COMP_{IN}$ (only the sign of the phase error will change). Thus, the exclusive-OR is not frequency-sensitive, but solely phase-sensitive.

With no loop filter, the output of the PC1 comparator will either raise or lower the VCO frequency arbitrarily, and the loop is likely to stay unlocked, see Fig.15(a). However, with a loop filter, the VCO output will be frequency-modulated. Since the SIG_{IN}frequency ($f_{SIG\ IN}$) equals $f_{VCO} - f_e$, the multiplication of both signals in PC1 produces a DC voltage which is accumulated by the integrating low-pass filter. If $f_{SIG\ IN}$ is lower than f_{VCO}, this voltage is negative, driving f_{VCO} towards $f_{SIG\ IN}$. Conversely, if $f_{SIG\ IN}$ frequency is higher than f_{VCO}, f_{VCO} is driven away from $f_{SIG\ IN}$. As the VCO frequency approaches the SIG_{IN} frequency, the DC level increases until lock is achieved as shown in Fig.15(b).

Noise sensitivity

The PC1 comparator is very insensitive to noise as can be seen in Fig.16. The average output voltage is hardly altered by the spike which will usually be removed by the filter.

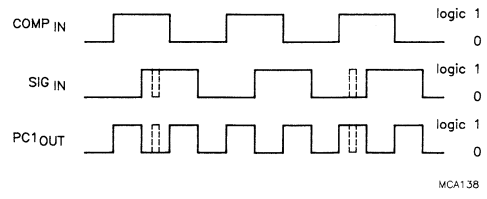


Fig.16 The PC1 comparator is very insensitive to phase noise.

Ripple frequency

Owing to the EX-OR operation of PC1, there is a ripple on its output of twice the input frequency and of 50% duty factor (typ.). Since the ripple frequency is rather high, it is easily suppressed by the low-pass filter.

Backlash

Backlash can only arise in sequential phase detectors, so not in PC1. Backlash is discussed in the section on PC2.

Free running frequency

With no input signal, the output frequency of PC1 is the same as that of the comparator input, $COMP_{IN}$. And because its duty factor is 50%, the average output voltage is $0.5V_{CC}$ which sets the VCO to its centre frequency f_0. So, even with no input signal, the VCO input is kept within the VCO's operating area without any clamping circuitry.

Conversion gain

The operating range of PC1 (0° to 180°) and the corresponding output voltage swing of V_{CC} means that the conversion gain, K_d, for input signals with a duty factor of 50% (and of other values) is:

$$K_d = V_{CC}/\pi \quad \text{V/rad.} \qquad (2)$$

Although K_d is independent of duty factor, as already explained, the lock-in range, hold range, pull-out and pull-in ranges are reduced for duty factors other than 50%.

Phase comparator 2 (PC2)

This is the most commonly-used phase comparator. It is a positive edge-triggered phase and frequency detector, comprising two D-type flip-flops, control gating and a 3-state output stage, see Fig.17. Since it is edge-triggered, the duty factor of the input signals is (unlike the PC1) unimportant.

Function

The circuit functions as a 3-state up-down counter where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count.

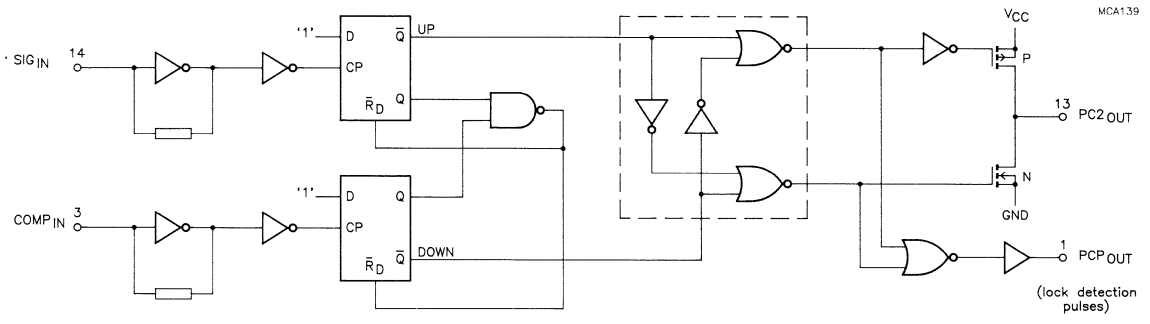


Fig.17 Logic diagram of a PC2 comparator. The two inverters and NOR-gates (boxed) prevent simultaneous conduction of the 3-state output transistors.

If the frequencies of SIG_{IN} and $COMP_{IN}$ are equal, but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-channel output driver is held on for a time corresponding to the phase difference. When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-channel driver is held on, see Fig.18. In Fig.18(a), the positive output pulses increase the VCO frequency until the phase error, ϕ_e, is zero, while in Fig.18(b), the negative pulses reduce the VCO frequency.

If the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-channel output driver is held on for most of the input signal cycle, and for the remainder of the cycle both n- and p-channel drivers are off (3-state). Conversely, if the frequency of SIG_{IN} is lower than that of $COMP_{IN}$, the n-channel driver is held on for most of the cycle. Therefore, the voltage on the filter capacitor C2, connected to $PC2_{OUT}$, varies until the signal and comparator inputs are equal in phase and frequency, see Fig.19. To obtain this characteristic with the PC1 or PC3 comparator, an active loop filter is required. Therefore, even with a passive filter, PC2 can be regarded as a phase comparator with an ideal integrator. This is discussed further in Appendix A.

When locked, the PC2 output is in its high-impedance 3-state. In a locked loop, there is no phase difference between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO.

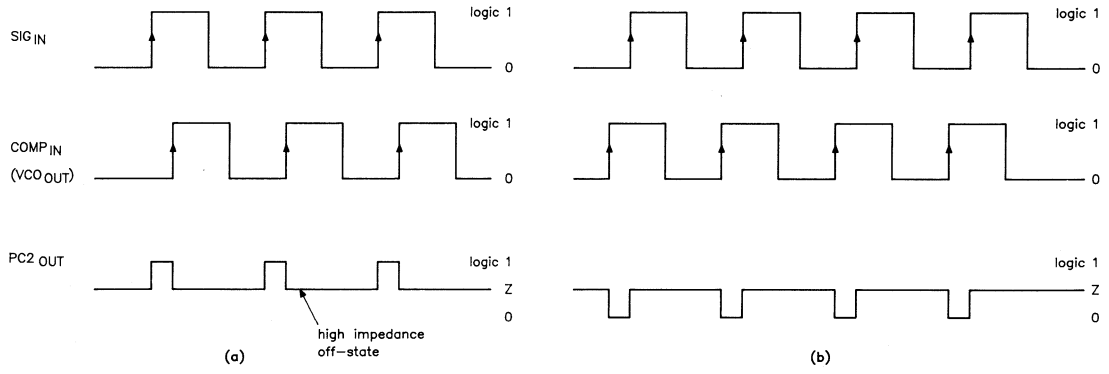
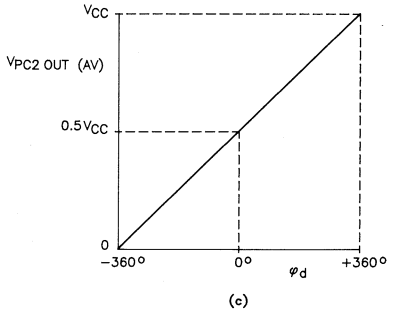
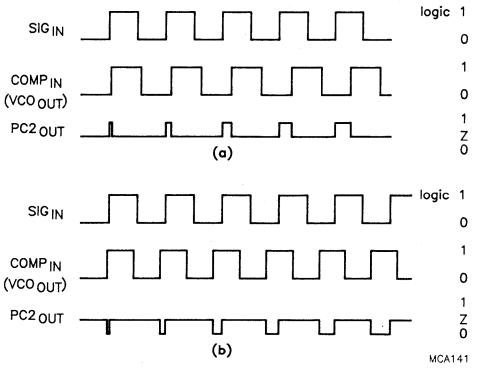


Fig.18 PC2 phase adjustment. (a)A rising edge of SIG_{IN} causes the p-channel driver to conduct until the next rising edge of $COMP_{IN}$ resets the output in the 3-state condition. (b)If the rising edge of $COMP_{IN}$ leads that of SIG_{IN}, the n-channel driver is switched on until the next rising edge of SIG_{IN} resets the output. (c) Average output voltage as a function of input phase difference.



MCA140



MCA141

Fig.19 PC2 frequency adjustment. Regardless of the frequency difference between SIG_{IN} and $COMP_{IN}$, although it must be in the operating range of the VCO, the PC2 comparator will always be able to adjust the VCO towards the input frequency. (a) frequency of SIG_{IN} initially higher than $COMP_{IN}$; (b) frequency of SIG_{IN} initially lower than $COMP_{IN}$.

Noise sensitivity

Unlike the PC1 comparator, PC2 is sensitive to phase noise, see Fig.20, and requires signals with a signal-to-noise ratio of typically >30 dB to operate correctly.

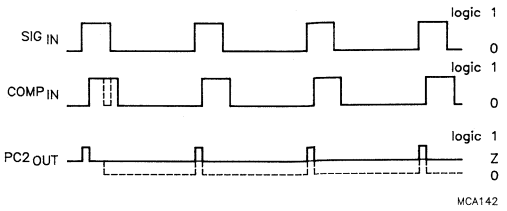


Fig.20 Unlike the PC1 comparator, the PC2 comparator is sensitive to phase noise. Just one extra transition of the input signal (dotted line) can produce a 2π phase error.

Ripple frequency

Ideally, when the PLL is locked, the comparator output remains in the 3-state condition and the filter capacitor voltage is constant. However, because filter capacitor C2, the 3-state output and the VCO input are not ideal, they sink or source a small leakage current, altering the capacitor voltage, and hence the VCO frequency, a little. This causes the comparator output to generate small correction pulses intermittently, however, the PLL is still considered to be locked. The frequency of these pulses (ripple frequency) is never higher than the input frequency. The amplitude of the sidebands produced is typically much lower than for PC1, because of the smaller duty factor of the ripple frequency.

Backlash

Owing to internal delays, the phase comparator needs a minimum phase difference between SIG_{IN} and $COMP_{IN}$ to generate an output pulse. This minimum phase difference is called the backlash time or dead zone, and is specified in seconds. The advanced design of the HCMOS comparator restricts the total backlash time to 2 ns (typ.), 4 ns (max.).

Phase and frequency jitter considerations

The intrinsic parasitic capacitances of the PC2 output (C_{par}, about 10 pF) widen the output correction pulses by an amount dependent on the RC time-constant, see Fig.21. With a 5 kΩ loop filter resistor, the pulse width is already about 50 ns longer than it should be, adjusting the phase error more than needed. At the next sample point, the same effect occurs, but in reverse, introducing phase jitter which, for video monitor applications in particular, is unacceptable. In addition, if the discharge time is long relative to the period of the input frequency, the actual output pulse width bears no relationship with the phase error anymore. This situation can be avoided by selecting the lowest allowable value for R3 (450 Ω), which reduces the discharge time to about 4.5 ns, allowing proper operation over the whole VCO frequency range.

The phase jitter can be eliminated by connecting a resistor, R_p, between the output of PC2 (pin 13) and GND such that the leakage current through R_p compensates, within one period, for the surplus charge injected by the parasitic output capacitance. The value of R_p is:

$$R_p \geq \frac{1}{3 \times 10 \times 10^{-12}(V_{CC} - 1)f_{in}} \quad \Omega. \qquad (3)$$

where V_{CC} is in volts, f_{in} in Hz.

The factor 3 in the denominator ensures that only positive correction pulses are generated even for the largest parasitic capacitances.

Discharging the parasitic capacitance to 1 V ensures that all surplus charge is compensated, but produces a very small, constant, phase difference between the input signal and the VCO output. In virtually all applications, this difference is not important.

If C2 is much larger than C_{par}, although there will be no jitter, another effect due to the parasitic capacitance, and the backlash, is to low-frequency-modulate the VCO output. When the VCO frequency moves slowly away from the input frequency, at least the backlash time (2 ns) is required before PC2 generates an output pulse. So, the parasitic capacitance is also charged, altering the voltage on the filter capacitor (C2) by:

$\Delta V_{C2} \approx \Delta V_{PC2OUT} C_{par}/C2$.

This in turn alters the VCO frequency by $\Delta f \approx \Delta V_{C2}$ VCO gain/2π.

The number of input cycles (n) needed before the delay between the rising edges of SIG_{IN} and $COMP_{IN}$ is again 2 ns (backlash time), but with opposite polarity, is:

$$n = \frac{\text{twice the total backlash time (4 ns)}}{1/f_{in} - 1/(f_{in} + \Delta f)}$$

The modulation frequency is $f_{in}/2n$, and depends solely on C2, the backlash time, the VCO gain, and the input frequency, so it cannot be filtered out. Increasing C2 will only decrease the modulation frequency. The way to avoid modulation is to add a leakage resistor as described, which biases PC2 away from its dead zone.

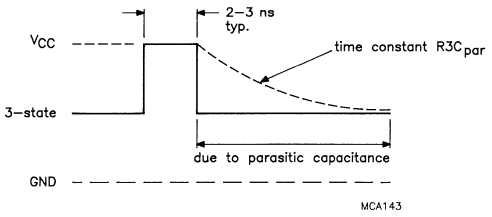


Fig.21 Widened pulse due to the 10 pF parasitic capacitance of the comparator output and the loop filter resistor R3.

Free running frequency

With no input signal, the positive transitions of the VCO set the comparator output LOW and discharge the filter capacitor. However, the time-constant of the loop filter is normally large enough to keep the VCO input voltage within the linear operating range. When it isn't, the VCO output frequency will either be f_{off}, or a few Hz as described in 'VCO linearity'. If this is not acceptable in the application, control voltage clamping must be used, see 'Application examples'.

Conversion gain

Since the comparator has an operating range of ±360° (±2π) and an output voltage swing of V_{CC}, the conversion gain if an active filter is used is:

$K_d = V_{CC}/4\pi$ V/rad. (4)

A filter with a resistor voltage clamp will reduce the effective output swing of the comparator, reducing the conversion gain, see 'Application examples'.

When a passive filter is used with PC2, the phase comparator gain will vary with the average output voltage (VCO input voltage) and:

K_d = average output voltage/2π V/rad. (5)

For a V_{CC} of 5 V, the gain will vary from 1.1/2π to 3.9/2π, thus by about 3.5:1 over the VCO's operating range. Equation 5 is derived in Appendix A which also discusses the effect of the varying gain in more detail.

Phase comparator 3 (PC3)

Only the 74HC/HCT4046A has this phase comparator which is a positive edge-triggered SR flip-flop as shown in Fig.22. This comparator is less sensitive to phase noise than PC2, but still requires input signals with a signal-to-noise ratio larger than about 20 dB.

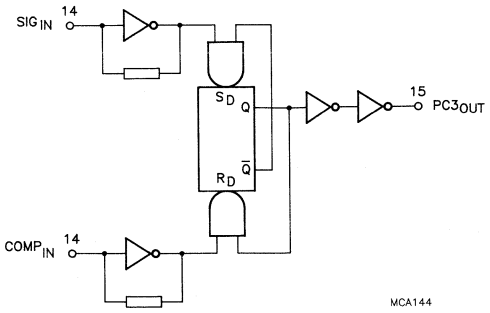


Fig.22 Logic diagram of the PC3 comparator

Function

Since PC3 is an edge-triggered comparator, the duty factors of SIG_{IN} and $COMP_{IN}$ are unimportant. A positive transition of SIG_{IN} sets the flip-flop and the push-pull output is HIGH. The next rising edge of $COMP_{IN}$ resets the flip-flop and the output is set LOW again. The average voltage on the the low-pass filter capacitor (which depends on the duty factor of the comparator output) adjusts the VCO accordingly.

Figure 23 shows phase adjustment using PC3 when both input frequencies are equal.

Figure 24 shows the situation when there is a frequency difference between SIG_{IN} and $COMP_{IN}$, along with the output signal which will adjust the VCO until both signals are equal in frequency. Figure 24(c) shows that when the difference is large, PC3 adjusts quickly, but takes longer to make the final adjustments as the VCO frequency appoaches the input frequency.

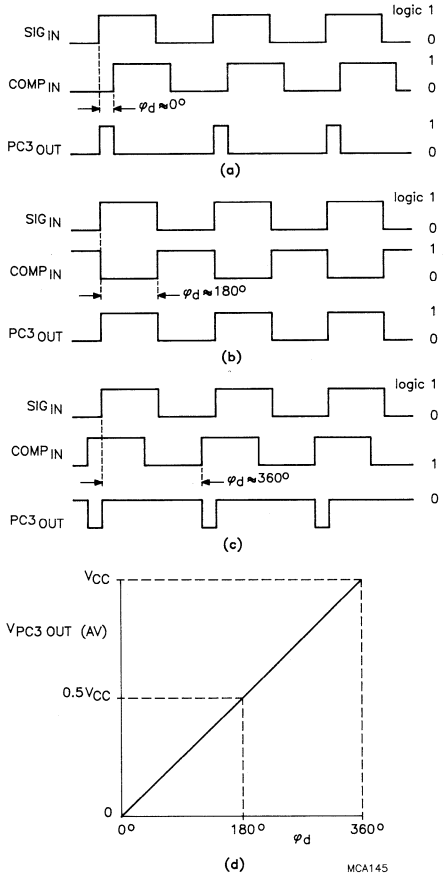


Fig.23 PC3 phase adjustment for input phase differences of (a) 0°, (b) 180° and (c) 360°. (d) Average output voltage as a function of input phase difference.

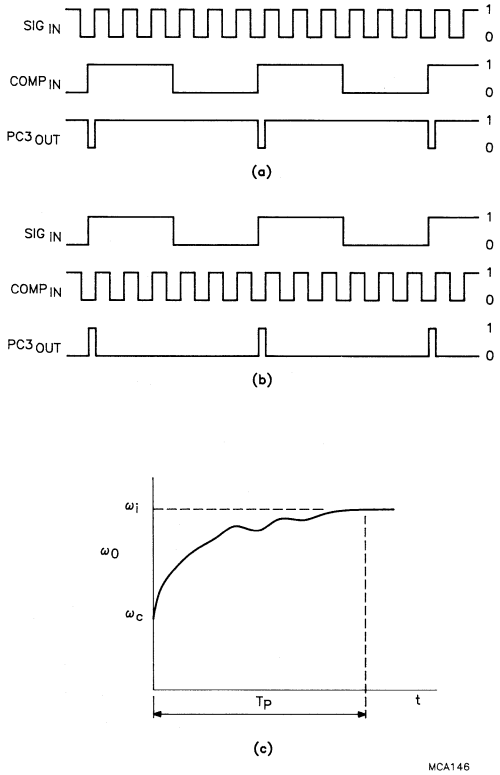


Fig.24 PC3 frequency adjustment.
(a) $SIG_{IN} > COMP_{IN}$; (b) $SIG_{IN} < COMP_{IN}$.
(c) Adjustment is fast initially, but slows down as the loop acquires lock.

A phase difference of 180° gives an average output of $0.5V_{CC}$ which sets the VCO at its centre frequency, f_0 (see Fig.23(b)). If the frequency of SIG_{IN} is not equal to f_0, the VCO needs to be adjusted, the phase difference between SIG_{IN} and $COMP_{IN}$ being increased or reduced depending on the frequency difference, until the average output voltage sets the VCO frequency to the SIG_{IN} frequency. The phase difference may vary between 0° and 360° but circuits are usually designed for a difference of about 180°, to give a symmetrical capture range. With PC3 and a passive filter, only the input frequencies are adjusted to be equal, no absolute phase relationship exists between the two input signals.

If an active filter is used, the phase difference remains at 180°, because the VCO input voltage is then generated by an integrator.

Noise sensitivity

The PC3 comparator is less sensitive to phase noise than PC2, see Fig.25.

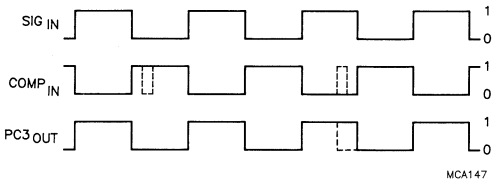


Fig.25 The PC3 phase comparator is less sensitive to phase noise than PC2.

Ripple frequency

The ripple frequency on the output of PC3 is the same as the input frequency, but with a duty factor of typically 50%. Since the output of PC3 swings by a greater amount than PC2 for input phase differences, and the duty factor is typically 50%, the ripple content of the output signal is higher than for PC2, requiring more filtering.

Back-lash

Since a typical loop using PC3 is designed to have a phase difference of 180° between SIG_{IN} and $COMP_{IN}$, the dead zone is usually on the edge of the operating area of the comparator (0° or 360°). Therefore, the effect on the performance of the comparator is unnoticeable.

Free-running frequency

The behaviour of PC3 is very similar to that of PC2. With no input signal, the output is set LOW, which discharges the filter capacitor.

Depending on the application, a voltage clamp may be needed to keep the VCO input voltage within range.

Conversion gain

The operating range of PC3 is from 0° to 360° and the output voltage swing is V_{CC}, which results in a conversion gain of:

$$K_d = V_{CC}/2\pi \quad \text{V/rad.} \qquad (6)$$

If a filter with a clamp is used, the effective output swing, and hence the conversion gain, will be smaller.

Lock detection indicator

It is sometimes convenient to have an indication of whether a PLL is locked. A lock detection indicator can be built for both HCMOS PLL circuits – the 4046A requiring some extra circuitry, the 7046A having this already built-in.

The lock indication is derived from the phase difference between SIG_{IN} and $COMP_{IN}$. Since the PC2 phase comparator has a phase difference of 0° over the entire VCO operating range, it is the easiest comparator for which to build a lock indicator. Of course, even when the PLL is locked, the VCO needs some small adjustments to stay locked, so the phase difference is not exactly 0°, but varies slightly depending on the loop parameters and the backlash time. The phase difference that is considered to represent 'out-of-lock' will depend on the application.

When the PC1 or PC3 comparator is used, together with a passive filter, lock-indication cannot be derived from the phase difference, because it can vary from 0° to 180° for PC1 and from 0° to 360° for PC3 (depending on the difference between f_0 and SIG_{IN}), while the loop is still considered to be locked.

Lock detector for the 74HC/HCT7046A

Figure 26 shows the circuit of the 7046A lock detection circuit.

When the PLL is locked, no pulses, or only very short pulses come from the up/down 'counter' of PC2. Any short pulses are removed by an RC filter and a Schmitt trigger produces a steady HIGH level at pin 1 (LD: lock detect) which indicates that the loop is locked, see Fig.27(a). If the up/down pulses are too long to be filtered out, the LD output will be pulsed LOW, indicating that the loop is out of lock (Fig.27(b)).

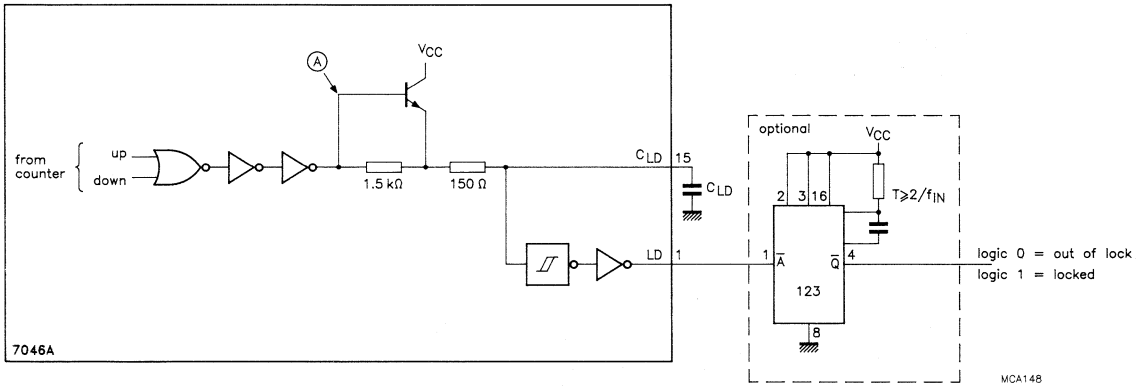


Fig.26 74HC/HCT7046A lock detection circuit. Adding a retriggerable monostable provides a steady-state lock indication.

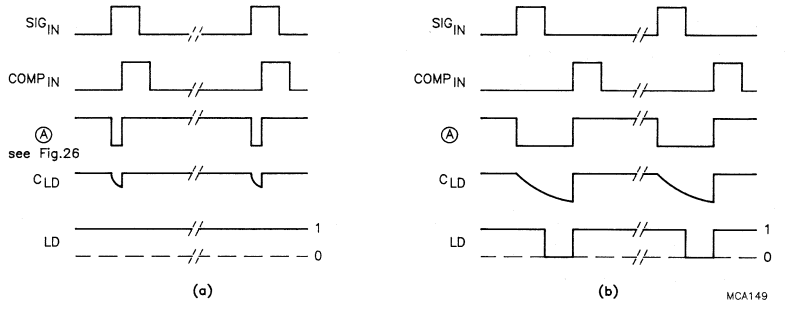


Fig.27 Lock detection waveforms. (a) locked; (b) out of lock.

The value of the external capacitor C_{LD} can be determined using Fig.28. First, define the maximum permissible phase error, ϕ_{max}, between SIG_{IN} and $COMP_{IN}$ for your application, then convert this into seconds using:

$$t_{LD} = \frac{\phi_{max}}{360} \times \frac{1}{f_{SIG\ IN}} \qquad (7)$$

Read off the value of C_{LD} from Fig.28.

With the addition of one retriggerable monostable (e.g. a '123', '423' or '4538'), a steady-state LOW and HIGH indication can be obtained, see dotted part of Fig.26. The pulse duration of the monostable must be longer than twice the period of the input signal (SIG_{IN}).

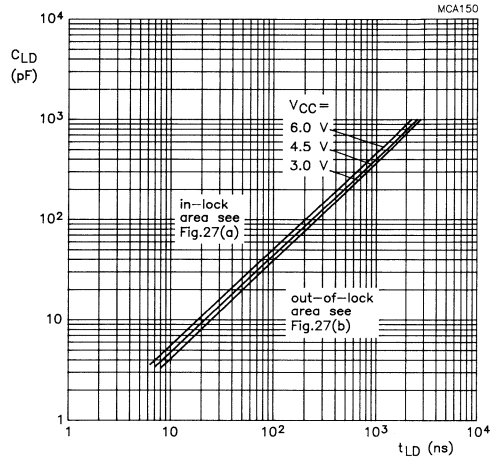


Fig.28 Graphs for determining the value of the capacitor C_{LD} connected to pin 15 to indicate a locked loop. Note, C_{LD} is the total capacitance at pin 15, i.e. the input capacitance of 3.5 pF, as well as the external capacitor. t_{LD} is the phase difference between SIG_{IN} and $COMP_{IN}$ positive-going edges.

Lock detector for the 74HC/HCT4046A

A very similar lock detection circuit can be built for the 74HC/HCT4046A using the PCP_{OUT} pin (pin 1), see Fig.29.

The waveforms shown in Fig.27 apply here too, only for signal A, read PCP_{OUT}. The same optional circuitry can also be used to obtain steady-state levels. In addition, since the PCP_{OUT} signal (the unfiltered output pulses from the phase comparator) is available with the 4046A, another circuit can be built using a D-flip-flop (74HC/HCT74) instead of the 74HC/HCT123 for better correlation with the maximum allowed phase error ($\phi_{e\ max}$) at higher frequencies (>5 MHz), see Fig.29.

To trigger a worst-case D-flip-flop, the pulse duation of each PCP_{OUT} pulse must be at least 16 ns (V_{CC} = 4.5 V) which sets the minimum t_{LD} at 16 ns too.

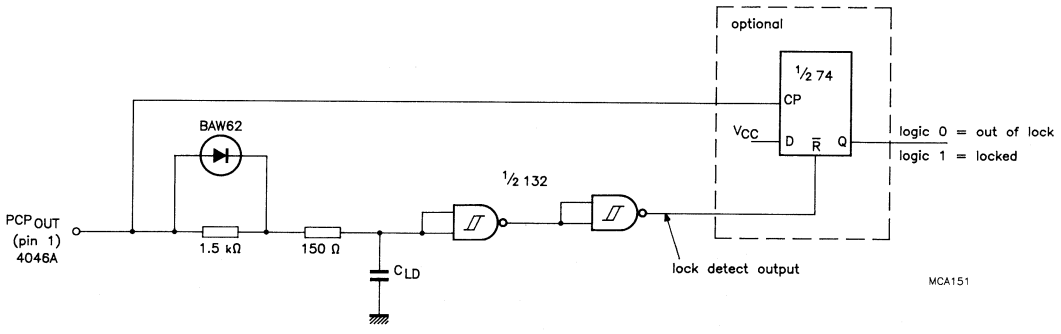


Fig.29 74HC/HCT4046A lock detection circuit. For a steady indication of lock, either the monostable circuit shown in Fig.26, or a D-flip-flop shown here can be added to the basic circuit.

Cycle slip detection

A signal can also be generated when the phase error exceeds 360° (cycle slip detection). Figure 30 shows a detection circuit suitable for all three phase comparators.

If two positive transitions occur on an input (SIG_{IN} or $COMP_{IN}$), while no positive transitions occur on the other, an output pulse is generated. This pulse can be used to trigger a monostable, for example.

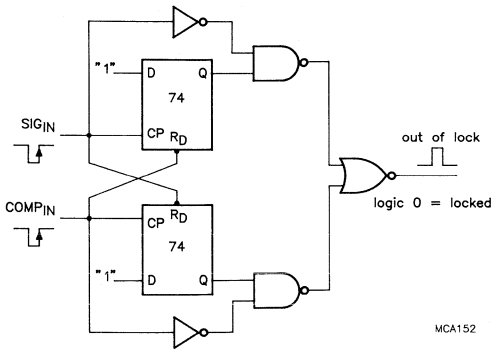


Fig.30 Cycle slip detection circuit suitable for PC1, PC2 and PC3.

Effect of temperature

The effect of ambient temperature on the frequency stability of the VCO has already been described. In this section, the effect of temperature on a complete, locked PLL is examined. The effect of temperature on the propagation delay of the phase comparators is the same as for standard HCMOS digital gates.

To recap for the VCO, if the ambient temperature increases, the VCO input voltage must be decreased to maintain a constant output frequency (Fig.11). In a closed loop, all three phase comparators will adjust the VCO in the desired manner to make the output frequency independent of temperature. However, with phase comparators PC1 and PC3, with a passive filter, to reduce the VCO input voltage, for example, the duty factor of the PC1 or PC3 output signal must be reduced to lower the average voltage on the loop-filter capacitor. Therefore, the absolute phase difference between SIG_{IN} and $COMP_{IN}$ will decrease too. This effect is absent when the PC2 comparator is used; its 3-state output goes LOW and stays LOW until the capacitor voltage is lowered sufficiently and the phase difference is zero again.

To summarize, the absolute phase difference between SIG_{IN} and $COMP_{IN}$ is temperature-dependent when PC1 or PC3 are used with a passive filter, and independent of temperature when PC2 is used. In addition, note that the VCO output frequency range is temperature-dependent. The phase difference variations when using PC1 or PC3 can be minimized by making the output frequency range of the VCO as wide as possible by raising the VCO conversion gain. They can be made completely independent of ambient temperature by using an active filter which has the same effect as using PC2.

Supply voltage

HC versions

Although the phase comparators of an HCMOS PLL can be regarded as standard digital circuitry requiring a supply voltage between 2 V and 6 V, the VCO section consists of several op-amps which need a supply voltage of at least 3 V. Therefore, the supply voltage range for the 74HC4046A/7046A is from 3 V to 6 V.

HCT versions

The 74HCT4046A and the 74HCT7046A are specified from 4.5 V up to 5.5 V supply voltage. The only other difference between the HC and HCT versions is the input level specification of the VCO inhibit input (pin 5).

HC and HCT versions

Slow variations of the supply voltage have no influence on the PLL output frequency when the loop is locked and stays within the operating range of the VCO. However, with PC1 and PC3, any changes in the VCO input voltage to keep the loop locked for a varying supply voltage will alter the phase difference between SIG_{IN} and $COMP_{IN}$, in a manner as described under 'Effect of temperature'.

Fast changes of voltage, or spikes on the VCO supply due to other logic circuits can influence the spectral purity of the VCO output frequency. Therefore, it is good practice to place decoupling capacitors as close as possible to the HCMOS PLL IC. For improved suppression of supply noise, connect a series inductor of say 100 µH between the normal digital supply and the V_{CC} of the IC. In addition, connect two capacitors (10 µF and 100 nF) between the V_{CC} of the IC and the GND pin for filtering.

Part-to-part spread

Both the 4046A and 7046A are manufactured using an advanced CMOS process with tight control of all process parameters to minimize part-to-part spreads. However, owing to the small spreads that remain, the output frequency of the VCO (set by R1, R2 and C1) can vary slightly from circuit to circuit. Although this variation can be eliminated by trimming R1 and R2, this is sometimes not desirable – for example, it's difficult with hybrid circuits. Some alternative methods are suggested below.

The part-to-part spread of an HCMOS VCO is ±20% for both the output frequency range ($2f_R$) and for the centre frequency (f_0). However, the spread in the maximum and minimum operating frequency (f_{max} and f_{min}) from circuit to circuit is limited, because circuits with maximum f_0 have a maximum $2f_R$. Similarly, those with minimum f_0 have a minimum $2f_R$.

There are three ways of determining suitable values for the external components (R1, R2 and C1) while guaranteeing that the input frequency is within the minimum $2f_R$ range:

- make the $2f_R$ range 20% larger than needed and trim the centre frequency to the desired value with R2;
- trim C1, which has the advantage that both the centre frequency and the $2f_R$ range can be adjusted to near their typical values;
- make the gain of the VCO, and hence $2f_R$, much larger than required for the application. Although the sidebands of the VCO output frequency will be increased when a divider is used in the loop, this can be compensated by lowering the natural frequency of the loop, ω_n, which will increase the settling time.

Figure 31 shows the effect of a ±20% part-to-part spread on the VCO operating range. In this example, f_0 equals $2f_R$.

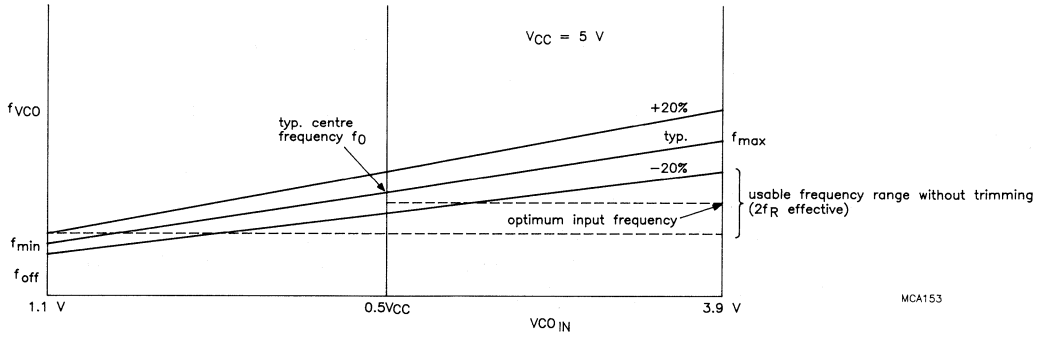


Fig.31 Effect of a 20% part-to-part spread on the VCO operating range.

Example

In the following example, the part-to-part spread (on VCO operating frequency) is assumed to be ±20% to which the tolerance of R1, R2 and C1 must be added. So, for 1% resistors and a 2% capacitor, the total spread is ±(20 + 1 + 1 + 2) = ±24%.

First, calculate the $2f_R$ required by the application, i.e. the effective $2f_R$ ($2f_{Re}$):

$$2f_{Re} = f_{max(typ)}(1-d) - f_{min(typ)}(1+d),$$
$$= 2f_{R(typ)} - 2df_{0(typ)}. \quad (8)$$

where $d = \frac{\text{spread in \%}}{100}$

Therefore, the typical $2f_R$ must be:

$$2f_{R(typ)} = 2f_{Re} + 2df_{0(typ)}. \quad (9)$$

The input frequency ($f_{SIG\ IN}$) is:

$$f_{in} = 2f_{Re}/2 + f_{min(typ)}(1+d)$$
$$= f_{0(typ)} - df_{R(typ)} \quad (10)$$

Therefore, the typical centre frequency must be at:

$$f_{0(typ)} = f_{in} + df_{R(typ)} \quad (11)$$

Because this value of centre frequency is slightly different to the original one, this new value should be inserted in Eq.(9), yielding:

$$2f_{R(typ)} = \frac{(2f_{Re}+2df_{in})}{1-d^2} \quad (12)$$

These values of f_0 and $2f_R$ ensure that the input frequency is always within the operating range of the VCO. In the PLL design program, they are calculated automatically from the specified input frequency and part-to-part spread.

The $2f_{R(typ)}$ just calculated can be so large that a negative offset is required. Since this is not possible, one has to trim one of the external components as mentioned earlier. For no offset, or positive offset:

$$f_{0(typ)} \geq 1.6f_{R(typ)}. \quad (13)$$

Power dissipation

For each phase comparator (VCO disabled), the power dissipation capacitance per package, C_{PD}, is 24 pF, and the power dissipation is:

$$P_D = C_{PD}V_{CC}^2f_{SIG\ IN} + C_LV_{CC}^2f_{PCP} + V_{CC}^2/4(R3+R4) \quad \mu W \quad (14)$$

where:

$f_{SIG\ IN}$ in MHz, C_{PD} in pF, V_{CC} in V, f_{PCP} in MHz, and R3 and R4 (R4 is in lag-lead loop filters, see Fig.34) in MΩ. Note that f_{PCP} is the frequency present at the PCP_{OUT} pin (4046A only); if this pin isn't used, $C_L = 0$, and the term $C_LV_{CC}^2f_{PCP}$ is zero.

In Eq.(14), it is assumed that the filter capacitor voltage is $0.5V_{CC}$ (typ.) and that the ripple is sufficiently suppressed by the filter. When the PC2 comparator is used, the last term of Eq.(14) can be neglected, because when the PLL is locked, the PC2 output is almost continuously in the high-impedance off-state, which significantly reduces the dissipation.

The contribution of the VCO section to the total dissipation is shown in Fig.32.

When a 4046A is used, the contribution of the PCP_{OUT} pin depends on the number of transitions. A worst-case approach is to make the number of transitions equal to $f_{SIG\ IN}$.

When a 7046A is used, the dissipation of the lock detect circuit and the C_{LD} capacitor is insignificant when the loop is locked, and is therefore not included in the calculations or dissipation graphs.

The total dissipation of the phase locked loop is the sum of all the individual values obtained from Fig.32 and Eq.(14).

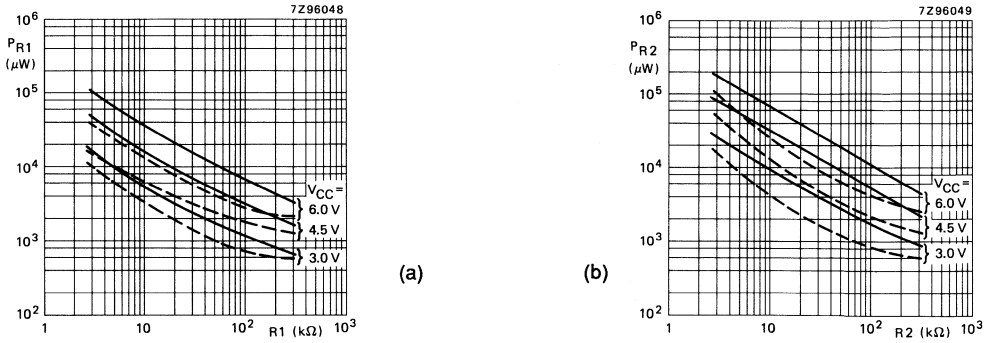
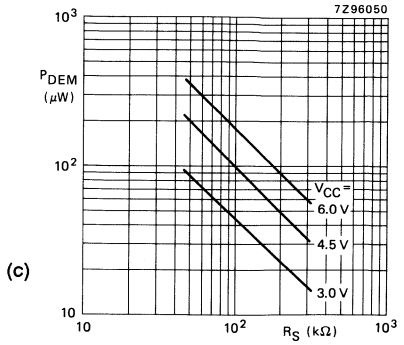


Fig.32 (a) Typical power dissipation of the VCO section as a function of resistor R1.
C_L = 50 pF; R2 = ∞; $V_{VCO\ IN}$ = 0.5V_{CC}; T_{amb} = 25 °C.
(b) Typical power dissipation of the VCO section as a function of resistor R2. C_L = 50 pF; R1 = ∞; $V_{VCO\ IN}$ = GND = 0 V; T_{amb} = 25 °C.
(c) Typical DC power dissipation of the demodulator section as a function of resistor R_S. R1 = R2 = ∞; T_{amb} = 25 °C.



PLL ANALYSIS

The capture process for a PLL is highly complex and does not lend itself to simple mathematical analysis. A locked PLL, however, can be approximated as a linear control system and analysed using Laplace transform techniques. In fact, most PLLs are designed using these techniques. In this section, the basic equations that describe a PLL are derived together with several graphical methods of evaluating the loop performance. The equations are basically those used in the PLL design program, and can be used to design a PLL manually, but are presented here to assist those using the program. In addition, the transient response and stability of a PLL are discussed.

Basic feedback system

Figure 33 shows a basic feedback system. From this figure, the closed-loop transfer function, H(s) is:

$$H(s) = \frac{A(s)}{1 + A(s)B(s)} \quad (15)$$

where:
s is the Laplace operator;
A(s) is the product of the feed-forward (i.e. open-loop) transfer functions;
B(s) is the product of the feedback transfer functions.

The error response is:

$$H_e(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{1}{1 + A(s)B(s)} \quad (16)$$

For a PLL,

$$A(s) = \frac{K_o K_d F(s)}{s}, \quad (17)$$

where:
K_o is the VCO gain;
K_d is the phase comparator gain;
F(s) represents the low-pass filter.

In Eq.(17), K_o is divided by s, because the frequency of the VCO output is converted to phase at the input of the phase comparator.

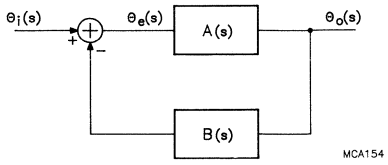


Fig.33 Feedback system. $\theta_i(s)$ = phase input; $\theta_o(s)$ = phase output; $\theta_e(s)$ = phase error; A(s) = product of the feed-forward transfer functions; B(s) = product of the feedback transfer functions.

In many applications, B(s) = 1, which represents a unity-gain feedback. In some applications, e.g. in frequency synthesis, see 'Application Examples', a divider (divide-by-N counter) is put in the feedback path between the VCO and phase comparator, and B(s) = 1/N. In these cases, the VCO operates at N-times the input frequency.

Loop filters

If the dynamic response of a system can be described by an nth-order differential equation, the order of the system is said to be n. If the transfer function of a (first-order) filter, F(s), is inserted in Eq.(17) and A(s) inserted in Eq.(15), the order of the transfer function H(s) of the complete PLL, and that of the error function, is two. In other words, the order of the PLL is the order of the loop filter plus one. If F(s) = 1 (no filter), the PLL is first order.

Because second-order PLLs are by far the most commonly used, only these are dealt with here. Second-order PLLs behave in a similar way to an RLC resonant circuit.

Of the many loop filters that can be used, only those shown in Fig.34 will be examined in the following section.

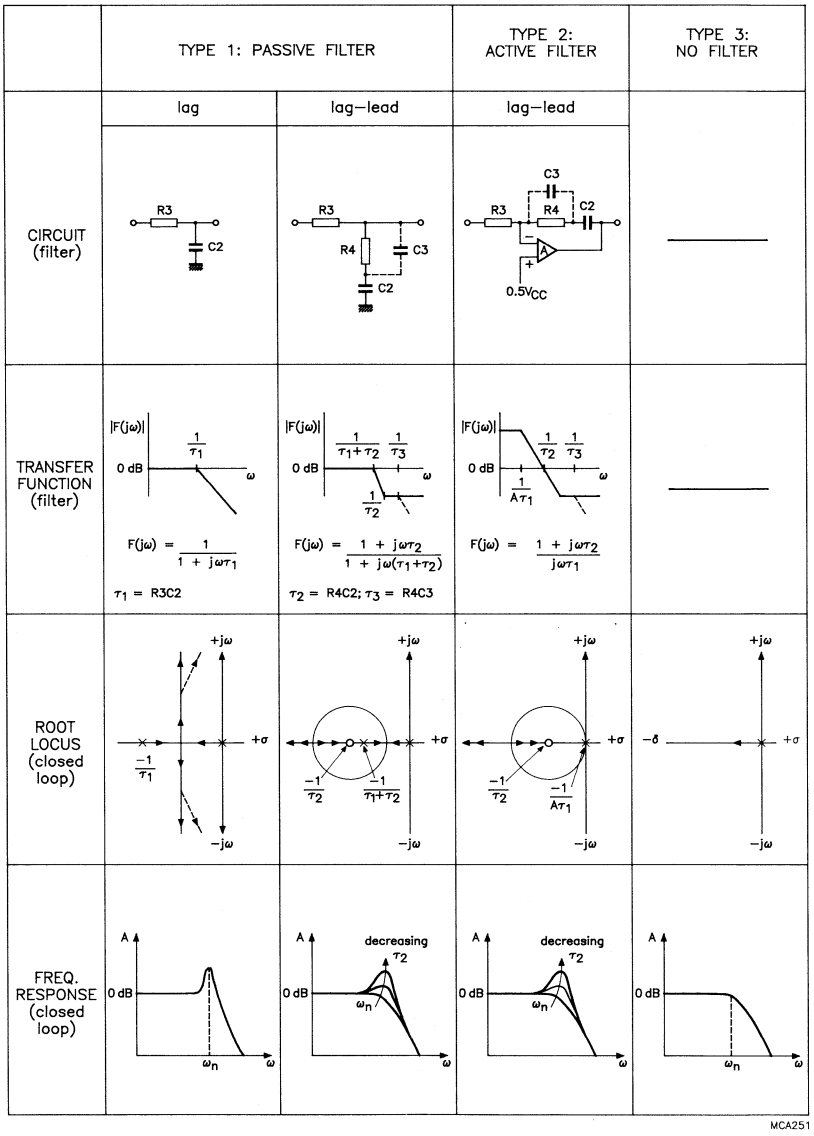


Fig.34 Some first-order low-pass filters and their transfer functions. The identification of resistors and capacitors is in accordance with Fig.3. The root-locus plots and frequency response curves are described on page 29. A zero-order filter (no filter) is included for completeness.

Second-order loop

As previously mentioned, to obtain the closed-loop transfer function, H(s), of a second-order PLL, the transfer function of the loop filter must be inserted in Eq.(15). Because the lag filter is a special case of a lead-lag filter with $\tau_2 = 0$, only the transfer functions of loops with lead-lag filters are calculated below.

For a PLL with an active loop filter:

$$H(s) = \frac{K_o K_d(s\tau_2 + 1)/\tau_1}{s^2 + s\frac{(K_o K_d \tau_2)}{\tau_1} + \frac{K_o K_d}{\tau_1}} \quad (18)$$

For a PLL with a passive loop filter:

$$H(s) = \frac{K_o K_d(s\tau_2 + 1)/(\tau_1 + \tau_2)}{s^2 + s\frac{(1 + K_o K_d \tau_2)}{\tau_1 + \tau_2} + \frac{K_o K_d}{\tau_1 + \tau_2}} \quad (19)$$

To simplify the calculation, N was taken to be one, i.e. no divider in the feedback.

By making suitable substitutions, the denominators of Eqs.(18) and (19) can be written in the normalized form:

$s^2 + 2\zeta\omega_n s + \omega_n^2$

where:

ω_n is the natural frequency

ζ is the damping factor.

For the active loop, the substitutions are:

$$\omega_n = (K_o K_d/\tau_1)^{1/2} \quad (20)$$

and

$$\zeta = 0.5\tau_2(K_o K_d/\tau_1)^{1/2} \quad (21)$$

For the passive loop, they are:

$$\omega_n = \frac{(K_o K_d)^{1/2}}{(\tau_1 + \tau_2)^{1/2}} \quad (22)$$

and

$$\zeta = \frac{0.5(K_o K_d)^{1/2}(\tau_2 + 1/K_o K_d)}{(\tau_1 + \tau_2)^{1/2}} \quad (23)$$

These substitutions result in the following transfer functions:

for the PLL with active loop filter:

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (24)$$

for the PLL with passive loop filter:

$$H(s) = \frac{s\omega_n(2\zeta - \omega_n/K_o K_d) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (25)$$

If $\omega_n/K_o K_d << 2\zeta$, Eqs.(24) and (25) are the same and the loop with the passive filter is called a high-gain loop.

When a lag filter (Fig.34) is used, $\omega_n/K_o K_d = 2\zeta$, so the loop is always low-gain. In addition, for lag filters, good tracking (large K_V) cannot be combined with a narrow loop bandwidth (ω_n) which is sometimes required for noise suppression.

When an active filter is used, the PLL is always considered to be a high-gain loop. In practice, most PLLs are high-gain loops, and all equations in the remainder of this publication are for high-gain loops, unless stated otherwise.

Bode plot

Figure 35 is a Bode plot of the closed-loop transfer function of a high-gain second-order PLL. The frequency scale is normalized to the natural frequency ω_n, so the plot can be used with any second-order PLL system. The plot illustrates the low-pass characteristic of such a PLL – slow variations of the input frequency are followed by the output, but frequency changes beyond the –3 dB point of the filter are damped.

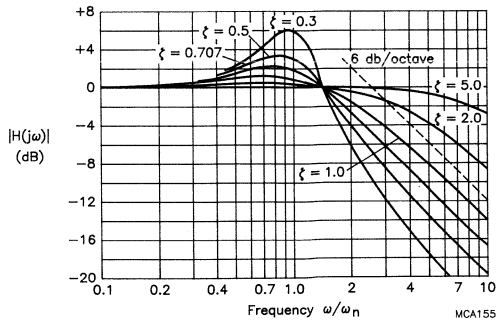


Fig.35 Closed-loop frequency response of a high-gain second-order PLL.

The Bode plot also illustrates that the damping factor, ζ, has a significant effect on the dynamic performance of the PLL:
when $\zeta = 1$, the system is critically damped;
when $\zeta < 1$, the transient response is oscillatory;
when $\zeta = 1/\sqrt{2}$, the transfer function is optimally flat and corresponds to that of a second-order Butterworth low-pass filter.

The −3 dB bandwidth (closed loop) is:

for a high-gain loop: $\omega_n[1 + 2\zeta^2 + (2 + 4\zeta^2 + 4\zeta^4)^{1/2}]^{1/2}$ (26)

for a low-gain loop: $\omega_n[1 - 2\zeta^2 + (2 - 4\zeta^2 + 4\zeta^4)^{1/2}]^{1/2}$ (27)

Root-locus plot

The roots of the denominator of Eqs.(24) and (25) are the closed-loop poles of the overall loop transfer function. The root-locus technique of determining the position of the system poles and zeros in the s-plane is often used to graphically visualize the stability of a system (Ref.1). The root-locus plot illustrates how the locus of the closed-loop poles varies with loop gain. For stability, all poles must lie in the left half of the s-plane. In general, the locus is drawn for the full range of gain variation – from zero to infinity. The plot starts (zero gain) on the open-loop poles and terminates (infinite gain) on the open-loop zeros.

The open-loop transfer function of any PLL is:

$K_V F(s)/s$ (28)

Thus, the open-loop poles always include one pole at the origin (due to the integrating action of the VCO) besides the poles of F(s) which represent the filter. The open-loop zeros are the zeros of F(s) and a zero at infinity due to the 1/s term.

The root-locus plots and the corresponding Bode plots for the passive filters are shown in Fig.34. For the simple lag filter, as the gain increases, the root loci bends as indicated by the dashed line owing to parasitic effects, and the poles move very close to the right half of the s-plane, indicating very little damping and that the loop is underdamped. This can happen if either the loop gain or the filter time constant is too large. Potential loop instability can be eliminated by using a lag-lead filter. When a leading term is introduced, (R4 in the filter), the poles also become complex when they meet, however, the complex portion of the locus is now a circle centred at $-1/\tau_2$ and which stays away from the right-half plane.

Another tool that provides information about the stability of a feedback system is the Bode plot of the open loop, which is described in the next section.

Phase and gain margin

A feedback loop can oscillate if its open-loop gain is unity and, simultaneously, its open-loop phase shift is 180°. A simple method of judging the stability of a PLL is the Bode plot of the open loop.

The easiest way to construct a Bode plot for a PLL is to plot the filter, $F(j\omega)$, separately from the VCO, phase comparator and feedback. Superposition of the individual plots yields the Bode plot of the complete (open) loop.

Passive filter

Figure 36 shows an example for a loop with a passive filter. The phase margin is measured at the frequency where the amplitude curve intersects the x-axis (0 dB value) and is the difference between the actual phase shift and −180°. The gain margin is measured at the frequency where the phase shift is −180° and is the difference between the actual gain and 0 dB. For second-order systems, the phase margin is of interest, because in virtually every application, it is the worst-case parameter to design. If the phase margin is small, say less than 20°, the loop will oscillate in response to a step input. To prevent this, a loop is normally designed to have a phase margin of 45° to 55°. As can be seen in Fig.36(a), a simple RC filter can result in very small phase margins if a large bandwidth is required.

If a zero is introduced in F(jω) by using a lag-lead filter, the phase margin can be increased to the desired value by varying τ_2, see Fig.36(b). Because of this zero, the PLL will act as a first-order loop at high frequencies, decreasing the noise and ripple suppression due to the phase comparator. Adding C3 will improve the suppression, but so as not to affect the phase margin, the additional pole introduced by C3 should typically be at $\tau_2/10$.

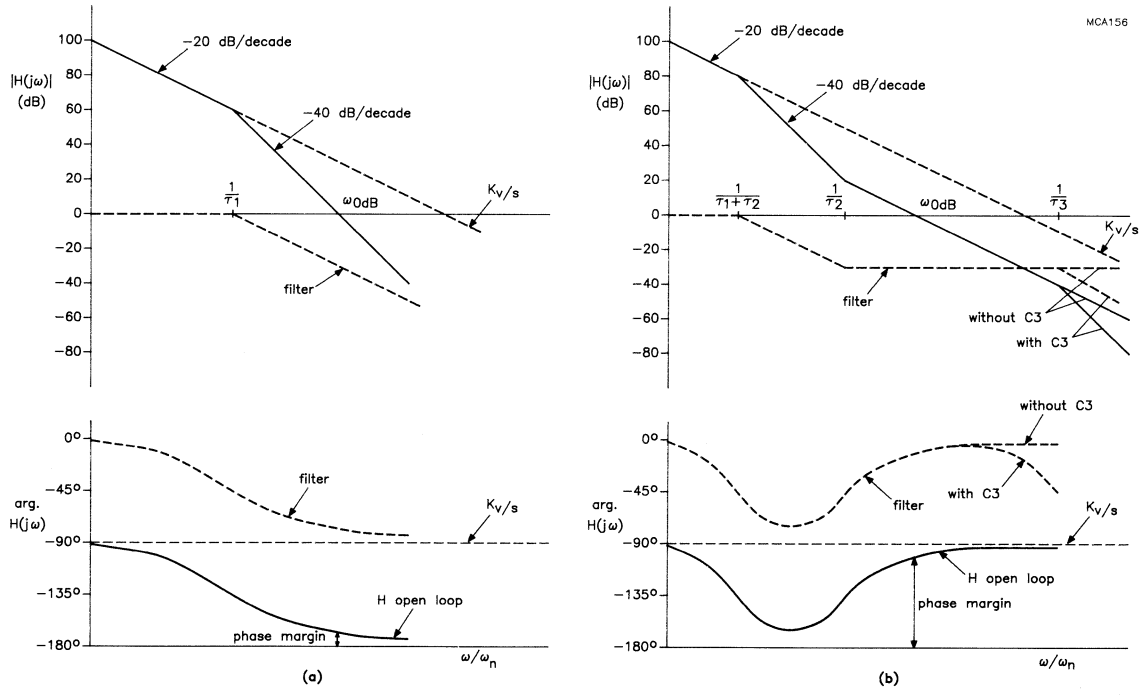


Fig.36 Bode plot of a PLL with (a) passive lag filter; (b) passive lag-lead filter. Refer to Fig.34 for filter types. Note, the decibel scales of the amplitude plots are not absolute and have been chosen for illustration only.

Active filter

For an active filter, the approach of positioning the additional pole is slightly different, see Fig.37. Only an active lag-lead filter is discussed, because an active RC filter will give an unacceptable phase margin of approximately 0°.

The first pole is at $1/A\tau_1$, where A is the open-loop gain of the filter's op-amp. Since A is very large ($>10^5$), this pole is nearly on the y-axis and the phase plot actually starts near −180° instead of −90°. The phase margin is now totally defined by τ_2, or by τ_2 and τ_3.

In Fig.37(a), the phase margin is determined by τ_2 alone, and τ_3 is located at $\tau_2/10$ as for the passive filter. If τ_3 is located closer to τ_2, the phase margin will be reduced, but the noise and ripple suppression will be increased, because the –40 dB/decade slope starts at a lower frequency. If τ_2 is moved to the left, the phase margin will be increased again. To simplify the positioning of τ_2 and τ_3, a special phase-lag network is used, see Fig.37(b) and Fig.38.

If τ_2 and τ_3 are positioned equidistant from $\omega_{0\,dB}$, the phase margin equals the difference between the maximum phase shift of this network and –180°. Figure 39 shows the maximum phase shift for this network as a function of τ_3/τ_2.

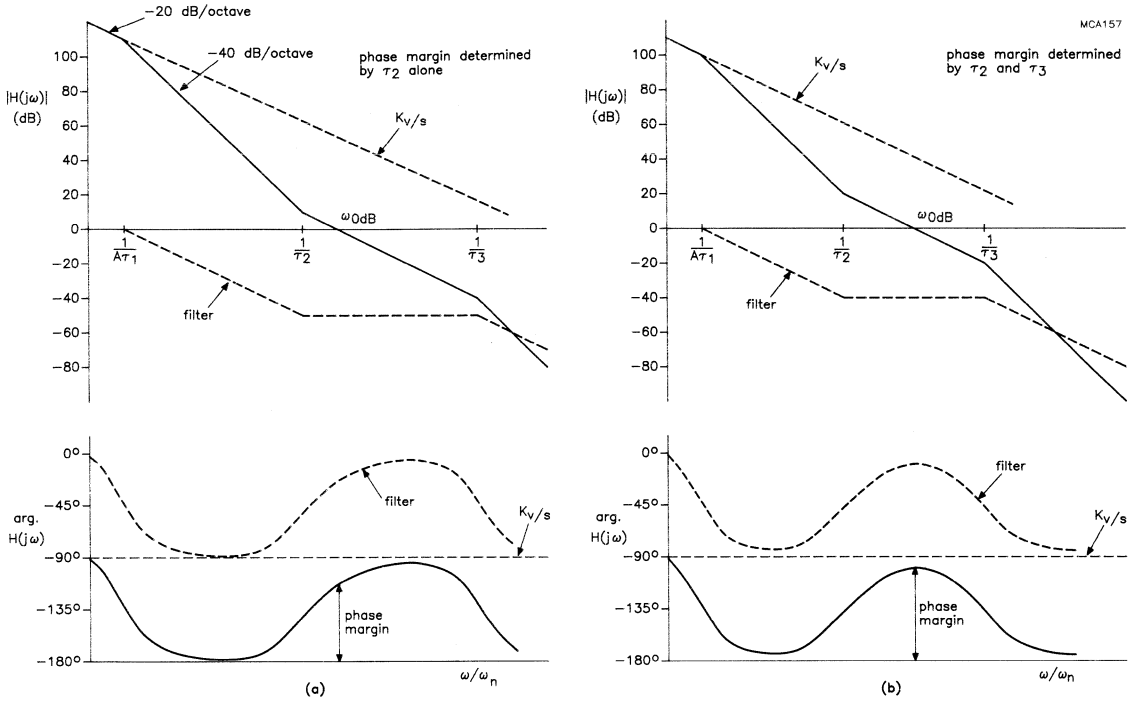


Fig.37 Bode plot of an active lag-lead filter (a) phase margin determined by τ_2; (b) phase margin determined by τ_2 and τ_3. Refer to Fig.34 for filter types. Note, the decibel scales of the amplitude plots are not absolute and have been chosen for illustration only.

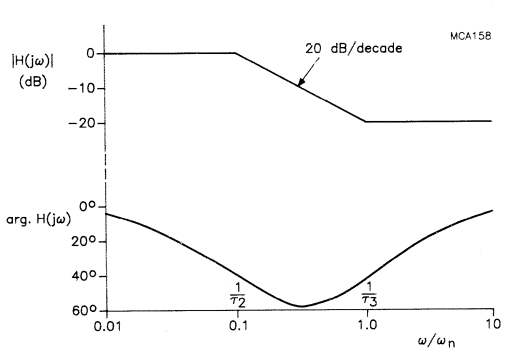


Fig.38 Phase and attenuation of a phase-lag network.

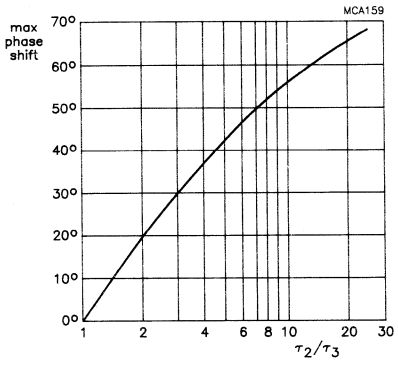


Fig.39 Maximum phase shift for a phase-lag network as a function of τ_2 and τ_3.

By using this method of defining the phase margin and positioning τ_2 and τ_3, both τ_2 and τ_3 are shifted to the left on the Bode plot and the amplitude roll-off starts earlier with the –40 dB/decade slope giving improved ripple and noise suppression.

As already discussed in the section on the PC2 comparator, the combination of PC2 with a passive filter results in a transfer function similar to that for when an active filter is used. The reason is that PC2 operates as a 'charge pump' (it's actually a voltage pump). The only disadvantage with the passive filter is the varying gain of PC2, see Appendix A. The first pole is now unlikely to be located at $1/A\tau_1$, since A was the open-loop gain of the filter op-amp. However, the open-loop gain of the op-amp can also be seen as the ratio of $R_o/R3$, where R_o is a resistor connected between the output of the op-amp and the inverting input. A value of A×R3 for R_o gives the maximum possible gain, or open-loop gain A. An equivalent situation occurs for PC2 with a passive filter. Now, 'A' equals the ratio between the leakage current of the capacitor C2 to that of R3, because the first pole is at $1/j\omega R_{leak}C = 1/\tau_1(R_{leak}/R3)$ (that is, at $1/'A'\tau_1$).

The resulting value of 'A' can be of the same order of magnitude as for an op-amp, resulting in a similar Bode plot.

Transient behaviour

An important characteristic of a PLL is its transient response to a frequency step or a phase step. This step can be a normal operating condition (for example, a FSK or PSK modulated input, frequency synthesizer) or an anticipated error condition. In both cases, it is necessary to know the overshoot as a percentage of the step, and the time when the output frequency or phase has resettled, say to within 5% of its end value.

A background to the validity of the graphs in this section is given in Appendix B.

Figure 40 shows the response of a low-gain second-order loop. The curves indicate both the phase response to a step in phase and the frequency response to a step in frequency. The curves are only valid for low-gain loops (passive filter), that is, where $\omega_n/K_oK_d > 2\zeta$, or $\tau_2 = 0$ (from Eq.(25)). The response of high-gain loops is shown in Fig.41. When $\omega_n/K_oK_d \approx 2\zeta$, or $\tau_2 \approx 0$, there is a gradual change from the curves of Fig.40 to those of Fig.41.

Figure 42 shows the phase response of a high-gain loop to a step in frequency. The phase error $\theta_e(t)$ approaches zero for large t. For low-gain loops using phase comparator PC1 or PC3, the curves are similar but the phase error does not decay to zero, but remains finite:

$$\theta_e(\infty) = \Delta\omega/K_oK_d \qquad (29)$$

where $\Delta\omega$ is the frequency step measured from the VCO centre frequency.

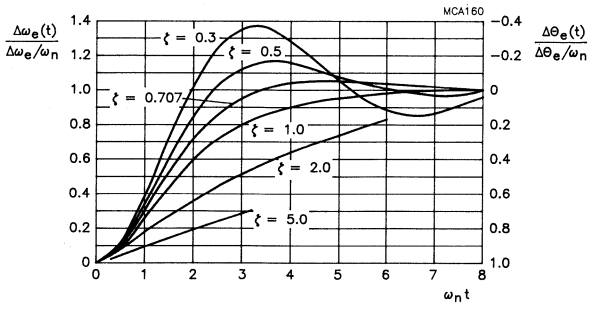


Fig.40 Step response of a low-gain loop.

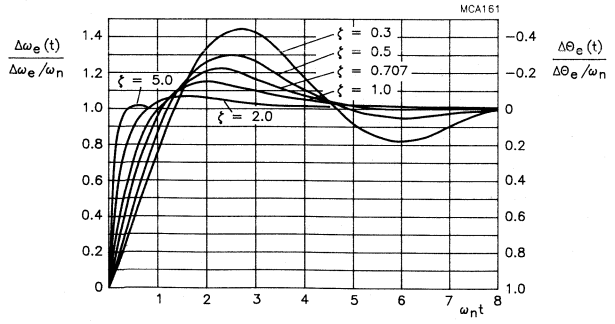


Fig.41 Step response of a high-gain loop.

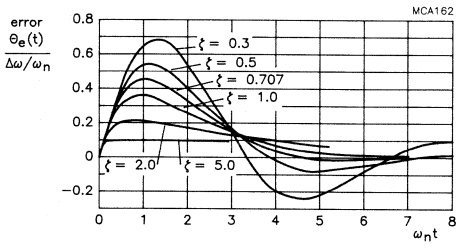


Fig.42 Phase response to a step in frequency.

Sinusoidally modulated input signal

The input signal can be sinusoidally modulated in frequency or in phase.

For phase modulation:

$$\theta_i(t) = \Delta\theta \sin \omega_m t \tag{30}$$

and for frequency modulation:

$$\theta_i(t) = \Delta\omega/\omega_m \cos \omega_m t \tag{31}$$

where $\Delta\theta$ is the peak phase deviation, $\Delta\omega$ the peak frequency deviation, and ω_m the modulating frequency.

The maximum amplitude of the phase error is obtained by multiplying θ_i by the magnitude of the error transfer function, $|H_e(j\omega_m)|$, see Eq.(16), yielding a peak phase error for phase modulation of:

$$\theta_e(\max) = \Delta\theta \frac{\omega_m^2}{\{(\omega_n^2 - \omega_m^2)^2 + (2\zeta\omega_n\omega_m)^2\}^{1/2}} \tag{32}$$

and for frequency modulation, of:

$$\theta_e(\max) = \Delta\omega \frac{\omega_m}{\{(\omega_n^2 - \omega_m^2)^2 + (2\zeta\omega_n\omega_m)^2\}^{1/2}} \tag{33}$$

For phase modulation with a fixed phase deviation, $\Delta\theta$, the phase error is small at low modulating frequencies, rises at 40 dB/decade and levels out at high frequencies to the value of the phase deviation, see Fig.43.

For frequency modulation with a fixed frequency deviation, $\Delta\omega$, the phase error is small at low modulating frequencies, rises to a maximum at $\omega_m = \omega_n$ and falls off at higher frequencies, see Fig.44. The asymptotes at low and high frequencies are 20 dB/decade.

For sinusoidal frequency-modulated input signals, it can be concluded that when $\omega_n \gg \omega_m$, the peak phase error is extremely small. And for sinusoidal phase-modulated input signals, make $\omega_n \ll \omega_m$ to demodulate the input signal with minimum distortion.

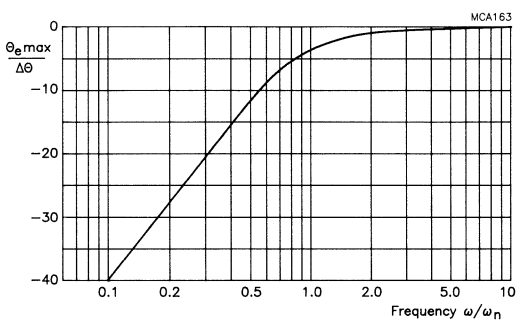


Fig.43 Peak phase error for a high-gain loop when phase modulated. $\zeta = 0.707$.

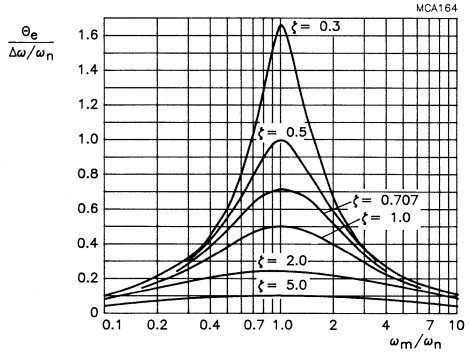


Fig.44 Peak phase error for a high-gain loop when frequency modulated.

Ripple suppression

An ideal phase comparator produces a DC signal which only varies when the phase difference between the inputs varies. Therefore, in a PLL with an ideal comparator, the low-pass filter would only be needed to suppress noise and to limit the maximum rate of phase changes seen by the loop. However, the HCMOS comparators PC1 and PC3 produce a pulsed output signal whose average DC value is related to the phase differences between the inputs. So, in an HCMOS PLL, the filter also has to average the signal from the phase comparator, and ideally fully suppresses the pulsed signal. The output of comparator PC2 is near ideal, but again the relatively short correction pulses won't be completely suppressed by the low-pass filter. Figure 45 shows the effect of the remaining ripple on the VCO output frequency for several values of division ratio N.

As already mentioned in 'HCMOS PLL circuits', the ripple frequency of PC1 is twice the input frequency, whereas the output frequency of PC3 and PC2 is equal to the input frequency.

When PC1 is used, the VCO output frequency will be modulated by the ripple of the phase comparator only if $N \geq 3$, generating sidebands in the spectrum of the VCO output spaced at multiples of the reference input frequency.

When PC3 is used, the duty factor of the VCO output frequency is affected by the ripple if $N = 1$. If $N > 1$, the output frequency is modulated by the ripple and sidebands are produced. In addition, since the Common Mode rejection Ratio of the op-amp used in the VCO is not infinite, sidebands will always be generated via the on-chip supply ripple, even if $N = 1$.

When PC2 is used, the output is modulated if $N \geq 1$. However, the sidebands produced will be much smaller than with PC1 & PC3 owing to the relatively small correction pulses. Since these pulses are both positive and negative, the sidebands will be spaced at half the input frequency. If a bias resistor, R_P, is used on the output of PC2 to compensate for the RC time constant of the parasitic output capacitance as described in 'Phase and frequency jitter considerations', the sidebands spaced at the reference input frequency will be dominant, because only the positive correction pulses appear on the output of PC2.

If it is assumed that the modulation index is low (i.e. ripple suppressed to a relatively low level), the level of the first sidebands (the only significant ones) can be calculated as follows.

The main component of the pulsed output of PC1 and PC3 is:

$$V_{ripple} \approx (2V_{CC}/\pi)\sin\omega_m t \qquad (34)$$

where ω_m is the modulation frequency.

This signal is damped by the filter, resulting in a ripple on the VCO input signal of:

$$V_{ripple(VCO)} \approx (2V_{CC}/\pi)\sin\omega_m t \times |F(j\omega)| \qquad (35)$$

where $|F(j\omega)|$ is the modulus of the filter (response) at $\omega = \omega_{ripple}$.
The VCO output frequency is:

$$VCO(t) = 0.5V_{CC}\cos(\omega_0 t + ß\sin\omega_m t) \qquad (36)$$

where:
$ß = (K_o 2V_{CC}/\pi f_m) \times |F(j\omega_{ripple})|$.
Since only the first sideband is assumed to be significant:

$$\text{sideband/carrier} \approx 20\log[(K_o V_{CC}/2\pi^2 f_m) \times |F(j\omega_{ripple})|] \quad dB \qquad (37)$$

Equation (37) is valid for rectangular output signals having a 50% duty factor. When the other sidebands cannot be neglected, it is only a very rough approximation of performance.

For PC2, the calculations are similar, yielding:

$$\text{sideband/carrier} \approx 20\log[K_o V_{CC}\tau \times |F(j\omega_{ripple})|] \qquad (38)$$

where τ is the width of the correction pulse. Note that Eq.(38) is also only an indication of performance, owing to the assumptions that have been made.

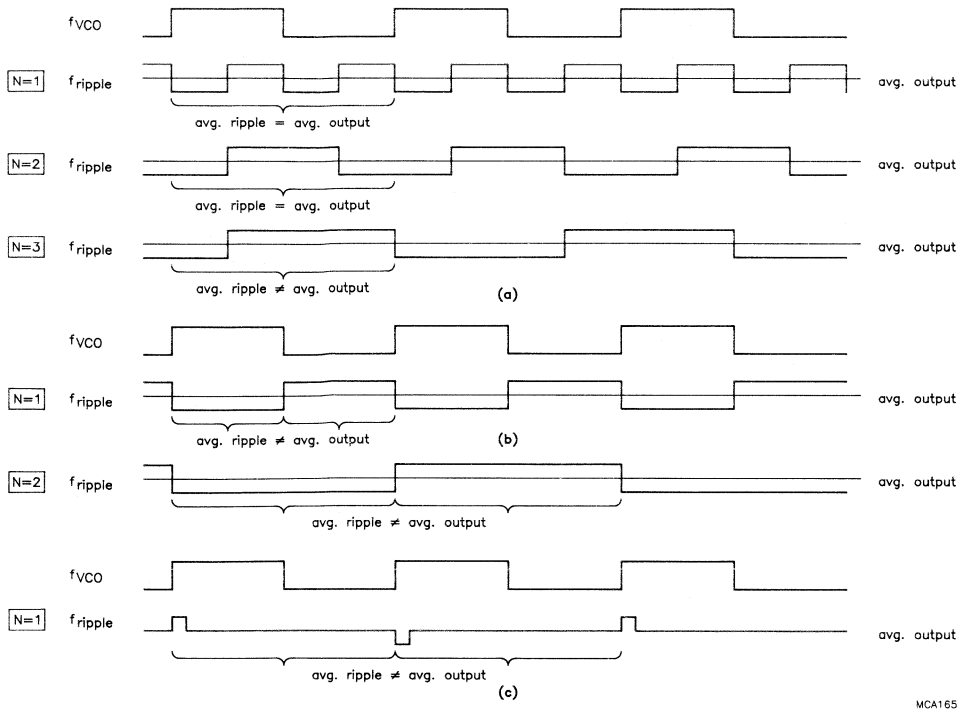


Fig.45 VCO output frequency, f_{VCO}, as a function of average ripple voltage; (a) for phase comparator PC1; (b) for PC3; (c) for PC2. N = division ratio.

Phase noise

If the signal-to-noise ratio of the input signal (SNR_i) is less than about 20 dB to 30 dB, only the PC1 comparator should be used, and then, SNR_i should still be >6 dB for correct operation. With PC2 and PC3, missing edges (due to noisy input signals) can cause incorrect operation, although if the missing transitions only occur occasionally, a fast settling time can be a remedy. PC3 is less sensitive than PC2 to missing transitions as described earlier. The remainder of this section applies to PC1 only.

Phase noise (jitter) on the VCO output signal is caused in part by noise on the input signal even though this is normally strongly attenuated by the PLL.

To calculate the signal-to-noise ratio of the VCO output frequency (SNR_o), it is necessary to know the SNR_i and the input noise bandwidth (B_i).

The actual phase jitter is:

$$(\Delta\varphi_i)_{RMS} = 1/2SNR_i \quad \text{rad.} \tag{39}$$

where SNR_i is expressed as a factor, and not in dB (10log SNR), as usually measured. And the SNR_o is:

$$SNR_o = SNR_i \times B_i/2B_L \tag{40}$$

where B_L is the noise bandwidth of the loop.
Thus, the PLL improves the SNR_i by $B_i/2B_L$, and:

$$B_L = 0.5\omega_n(\zeta + 1/4\zeta) \quad \text{Hz} \tag{41}$$

where ω_n is in rad/s.
Clearly, low values of ω_n will improve SNR_o, and the noise bandwidth is lowest for values of ζ between 0.5 and 1.

The phase jitter of the VCO output caused by the input noise equals:

$$(\Delta\varphi_o)_{RMS} = 1/2SNR_o \quad \text{rad.} \tag{42}$$

For PC1, the average time before the loop loses lock due to the input noise, and for $\zeta = 0.7$, is:

$$T_{AV} \approx (2/\omega_n)\exp(\pi SNR_o) \quad \text{sec.} \tag{43}$$

Overview of PLL parameters

Table 1 gives a summary of the most important design equations for a second-order PLL.

Table 1: The main design equations for a second-order PLL using a 4046A or a 7046A

	PC1	PC3	PC2
hold range $\pm\Delta\omega_H$	$2f_R$ (active filter); $\frac{\pi K_V}{2}$ (passive filter)	$2f_R$ (active filter); πK_V (passsive filter)	$2f_R$
lock-in range $\pm\Delta\omega_L$	$\approx \pi\zeta\omega_n$	$\approx 2\pi\zeta\omega_n$	$\approx 4\pi\zeta\omega_n$
settling time T_S	$\approx 1/\omega_n$	$\approx 1/\omega_n$	$\approx 1/\omega_n$
pull-in range $\pm\Delta\omega_{PI}$	$\approx \frac{\pi\sqrt{(2\zeta\omega_n K_V)}}{2}$	$\approx \pi\sqrt{(2\zeta\omega_n K_V)}$	$2f_R$
pull-in time T_P	$\approx \frac{4\Delta\omega_o^2}{\pi^2\zeta\omega_n^3}$	$\approx \frac{\Delta\omega_o^2}{\pi^2\zeta\omega_n^3}$	$\approx \frac{N\tau_1 + \tau_2}{K_o K_d^*}$
pull-out range $\pm\Delta\omega_{PI}$	$\approx 1.8\omega_n(\zeta + 1)$	$\zeta<1$: $\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{(1-\zeta^2)}} \frac{\tan^{-1}\sqrt{(1-\zeta^2)}}{\zeta}\right]$ $\zeta=1$: $\pi\omega_n \exp 1$ $\zeta>1$: $\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{(\zeta^2-1)}} \frac{\tanh^{-1}\sqrt{(\zeta^2-1)}}{\zeta}\right]$	$\zeta<1$: $2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{(1-\zeta^2)}} \frac{\tan^{-1}\sqrt{(1-\zeta^2)}}{\zeta}\right]$ $\zeta=1$: $2\pi\omega_n \exp 1$ $\zeta>1$: $2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{(\zeta^2-1)}} \frac{\tanh^{-1}\sqrt{(\zeta^2-1)}}{\zeta}\right]$

All parameters are related to the input of the PLL, and are valid for high-gain loops only.
N is the division ratio.
* $K_d = V_{CC}/\omega_{in}$ (out-of-lock gain)

PLL DESIGN PROGRAM

All the main parameters of a PLL can be calculated from the information in the previous sections, but it is clearly a time-consuming task when done manually. In addition, because most parameters are interdependent, all the calculations should be repeated every time a parameter is altered. Short-cuts taken to simplify the recalculation often result in non-optimum loop performance. To solve this problem, we have developed a computer program which as well as making all the necessary calculations fast, allows the designer to make modifications and to see their effect in a few seconds. The program runs on an IBM PC or compatible with MSDOS. A graphics card such as an EGA or Hercules card is helpful, but not essential. The program is suitable for use with three types of loop filter, see Fig.34:

- type 1 (passive) with or without C3;
- type 2 (active) with or without C3;
- type 3 (no filter) for FSK and PSK applications.

About the program

After some introductory text when you start the program, you'll come to a block diagram of a PLL showing the basic components. The main program starts by asking for system information such as input frequency, division ratio, supply voltage, and the type of phase comparator you wish to use. One of three application areas is then chosen depending on the division ratio and input frequency (see below, for more details):

- fixed division ratio, fixed input frequency.
  Examples: tracking filter, multiplier.
- fixed division ratio, modulated input frequency.
  Examples: FM, PM, FSK, PSK.
- variable division ratio, fixed input frequency.
  Example: frequency synthesizer.

Then the calculations start using default settings which will always produce a stable loop design. The results are presented in three groups, see Fig.46:

- the system parameters you specified
- the calculated values of the external bias components for the VCO, and the values of the loop filter components and constants
- the calculated dynamic loop parameters.

An extremely useful feature of the progam is the already-mentioned ability to tailor the loop parameters to specification quickly. After optimization, you can print the results.

```
                          INPUT PARAMETERS
PC      : 1       fin  (Hz) :  1.000E+05    Spread input freq.  (%) :  0.0
N       : 30.0    2fR  (Hz) :  2.897E+06    Part-to-part spread (%) : 32.0
Filter :  1       f0   (Hz) :  2.963E+06    Vcc              (Volt) :  5.0

                      VCO and FILTER PARAMETERS
T1 (sec) :  1.2E-03        T2 (sec) :  8.2E-05       T3 (sec) :  7.2E-06
f1  (Hz) :  1.2E+02        f2  (Hz) :  1.9E+03       f3  (Hz) :  2.2E+04
R1 (Ohm) :  1.5E+04        R3 (Ohm) :  4.4E+02       R4 (Ohm) :  3.0E+01
R2 (Ohm) :  1.3E+05        C2 (Far) :  2.7E-06       C3 (Far) :  2.4E-07
C1 (Far) :  1.0E-10

                        DYNAMIC PARAMETERS
Wn/2π                (Hz) :  2.6E+03  pull-in time          (sec) :  2.6E-03
W_0dB/2π             (Hz) :  4.4E+03  pull-in range          (Hz) :  2.2E+04
zeta                      :  0.70     pull-out range         (Hz) :  8.0E+03
overshoot             (%) : 21.03     hold range             (Hz) :  8.6E+04
Kv                        :  3.4E+05  settling time (<5%)   (sec) :  2.8E-04
Winput/W_0dB              : 22.7      lock-in range          (Hz) :  5.7E+03
phasemargin with C3 (deg) :  55       ripple suppr. with C3 (dB) : -23
         without C3 (deg) :  64                 without C3 (dB) :  -6
zetamin                   :  0.70     Wnmin/2π               (Hz) :  2.6E+03
zetamax                   :  0.86     Wnmax/2π               (Hz) :  3.2E+03
                                                    Philips Components
Optimize ? (Y/N): Y
```

Fig.46 Example of a 'result window'. The window lists all parameters which define the dynamic performance of the loop, and the filter components R3, R4, C2 and C3. In addition, the external components R1, R2 and C1 which set the free-running frequency of the VCO are calculated.

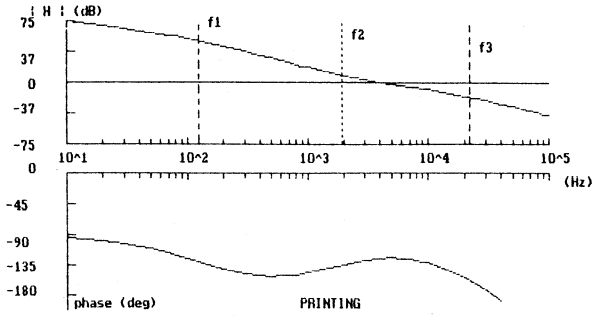


Fig.47 Example of an open-loop Bode plot generated by the design software. The corner frequencies f_1, f_2 and f_3 are indicated by vertical lines on the amplitude curve.

And if your PC has a suitable graphics card, you can generate a Bode plot of the open loop to examine the loop stability, see Fig.47, returning to the optimization menu to make further alterations to the design as required. One option in the optimization menu can be used to evaluate existing designs.

Hard copies of the results and the Bode plot can be made on an Epson or IBM printer, or compatible.

Initial PLL default settings

To ensure that the loop is stable, the program starts with a set of default values for parameters such as the damping factor and the phase margin. Other default values depend on the application area as follows.

Fixed division ratio and fixed input frequency

To obtain an acceptable ripple and noise suppression and a fast settling time, the natural frequency of the loop (ω_n) is set to an arbitrary value of $0.05\omega_{in}$.

The corner frequencies of the filter are determined differently depending on whether the filter is passive or active, as described under 'Phase and gain margin'.

For a passive filter, with the default value of ω_n and a default damping factor of 0.7 (Butterworth response), τ_1 and τ_2 are determined from Eqs.(22) and (23), K_o and K_d already having been determined from the $2f_R$ range of the VCO and the choice of phase comparator to be used respectively. If τ_1 or τ_2 falls below zero, ω_n is multiplied by 0.99 and the calculations are repeated. So as not to influence the phase margin, τ_3 is positioned at $0.1\tau_2$.

For an active filter, or when PC2 is used, a default of $\tau_2/\tau_3 = 10$ is used which gives a phase margin of about 55° (see Fig.39). First, $\omega_{0\ dB}$ is calculated with the default ω_n and the equation:

$$\omega_{0\ dB} = (\tau_2/\tau_3)^{0.25}\omega_n \qquad (44)$$

Both τ_2 and τ_3 are located symmetrically around $\omega_{0\ dB}$ by making:

$$\tau_2 = \sqrt{10}/\omega_{0\ dB} \qquad (45)$$

and

$$\tau_3 = 1/(\omega_{0\ dB}\sqrt{10}) \qquad (46)$$

τ_1 can be determined from:

$$|H(j\omega)| = 1 \text{ (open loop)} \qquad (47)$$

with $\omega = \omega_{0\ dB}$, yielding:

$$\tau_1 = \frac{K_v \times \{(1/\omega_{0\ dB}^2) + \tau_2^2 + \tau_3^2 + 2\tau_2\tau_3\}^{1/2}}{\omega_{0\ dB}[\omega_{0\ dB}^2\tau_3^2 + 1]^{1/2}} \qquad (48)$$

If $1/\tau_3 < 5\omega_n$, τ_1 and τ_2 are determined using Eqs.(20) and (21) and:

$$\omega_{0\ dB} = \omega_n[2\zeta^2 + (4\zeta^4 + 1)^{1/2}]^{1/2} \qquad (49)$$

$1/\tau_3$ is now positioned at $5\omega_n$.

Fixed division ratio, modulated input frequency

The default values of ω_n and the damping factor, ζ, depend on whether the input is sinusoidally modulated (FM, PM) or step modulated (FSK, PSK).

For sinusoidal frequency-modulated input signals, distortion is important, and to keep the maximum phase error small, ω_n should be much larger than the modulating frequency, ω_m, as Fig. 44 shows. An initial default value of $\omega_n = 100\omega_m$ is used.

For phase-modulated input signals, the initial default is $\omega_n = .01\omega_m$.

For FSK or PSK, the graphs of Fig.41 are used. A maximum overshoot or damping factor together with a settling time is used to determine ω_n. For example, a maximum overshoot of 21%, or $\zeta = 0.7$, results in an $\omega_n t$ of 1. If the output frequency or phase must settle within 1 ms (settling time), ω_n is 1/0.001 = 1000 rad/s.

If a passive filter is used, the calculations proceed as described under 'Fixed division ratio and fixed input frequency'.

For an active filter, or if PC2 is used, the factor τ_2/τ_3 must be calculated from ζ and:

$$\tau_2/\tau_3 = [\tan(\pi/4) - 0.5\arctan(2\zeta)]^2. \quad (50)$$

$\omega_{0\ dB}$ can be calculated from Eq.(44).
The remaining calculations are identical to those described in 'Fixed division ratio and fixed input frequency'.

Varying division ratio, fixed input frequency

Varying the division ratio or switching between channels introduces a frequency step at the phase comparator input. Therefore, the graphs of Fig.41 are used again to determine ω_n. In frequency synthesizer applications, the settling time is defined as 'when the output has setled to within 5% of the applied step. So, the value of $\omega_n t$ becomes 4.5 for $\zeta = 0.7$. Hence, if $T_{S(5\%)} = 1$ ms, ω_n becomes 4.5/0.001 = 4500 rad/s. In this case, ($\zeta = 0.7$), ω_n is four and a half times that value in the previous example owing to the different definition of settling time. Once ω_n has been determined, the calculations are identical to those described under 'Fixed division ratio, modulated input.'

Optimizing a loop

The program enables sixteen parameters, see Table 2, to be altered individually, the new values of the dependent parameters being calculated automatically. When a parameter is chosen, a 'general information and warnings' window is displayed which gives a description of the parameter and indicates which of the other main parameters will change if the selected parameter is changed. Next, the present value of the parameter is given after which the user can insert the desired value. With the program, a complete loop can be designed to your specification fast.

In the program, a loop is modified by altering one of the two main loop parameters, ω_n or ζ. Sometimes, this does not produce the desired result exactly, in which case, re-enter the value of the parameter to be altered (via the optimize menu), and re-optimize.

With certain loop configurations, e.g. with a particular phase comparator or filter, a warning is displayed when it is impossible to make the modifications requested. In these cases, it is suggested that the following be tried. If the 'General Information and Warnings' window mentions that ω_n has been altered to obtain the desired result, it may help to alter the other main loop parameter, ζ, using the optimize facility. For example, although the settling time depends on ω_n and ζ, in the optimize facility, a requested value of T_S is obtained by changing ω_n alone. If ω_n cannot be made large enough, T_S can be reduced by decreasing ζ.

Experimenting with the optimization stage is highly instructive and is recommended to gain insight into the behaviour of a loop and to observe how the different parameters interact.

Table 2: PLL parameters that can be optimized in the design program

0.	division ratio N, or max. phase error
1.	VCO output frequency range
2.	hold range
3.	phase margin
4.	ripple suppression
5.	settling time
6.	lock-in range
7.	pull-in time
8.	pull-in range
9.	pull-out range
10.	values of the filter components
11.	damping factor ζ
12.	natural loop frequency
13.	$\omega_{0\ dB}$
14.	overshoot
15.	ω_{-3dB}

the numbers correspond to those in the optimization menu.

Evaluating existing designs

The PLL design program enables existing designs to be evaluated and, if required, redesigned to upgrade system performance.

After the system information has been entered in the usual way, the program calculates the loop parameters using the default settings as previously described. The results and the Bode plot can be compared with those of the existing design. The filter components of the existing design can be entered using option 10 of the optimization menu, and the loop parameters recalculated by the program. These results and the Bode plot give the designer a complete insight into the performance of the loop. Finally, the loop can be optimized and a new set of loop components generated to upgrade the original design. If the existing filter is not one of the three types which the program can handle, see Fig.34, the filter transformations shown in Fig.48 may be helpful.

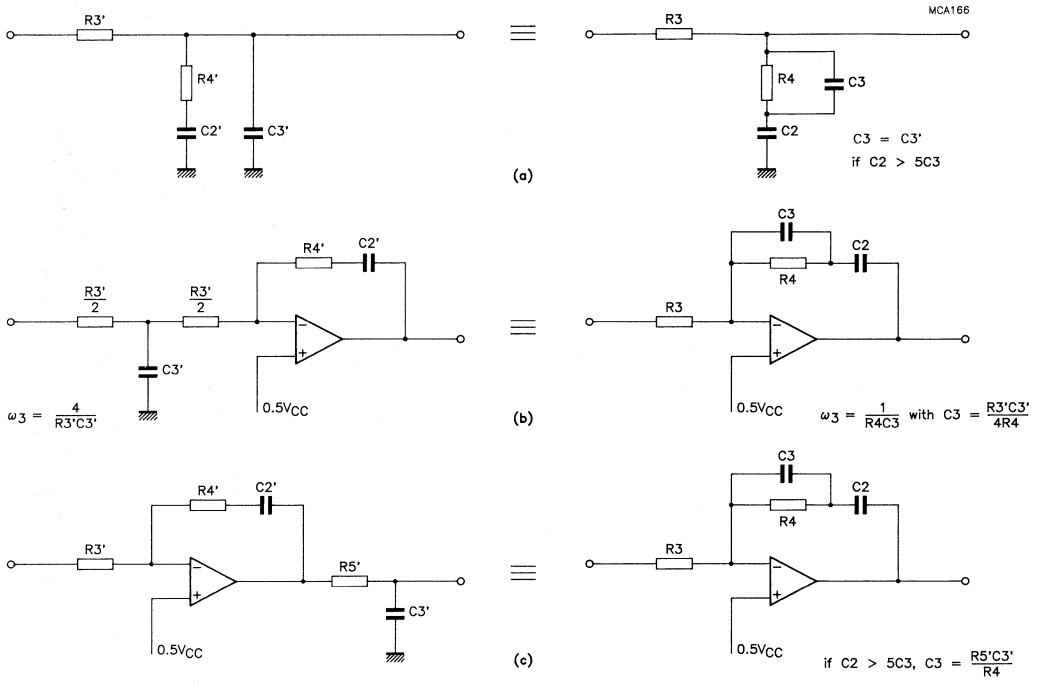


Fig.48 Filter transformations. (a) to a passive filter; (b) and (c) to an active filter.

APPLICATION EXAMPLES

Filter output clamping

In some applications, it is useful to clamp the filter output to prevent the VCO running too low or too high. For example, with phase comparators PC2 and PC3, when there is no input signal for a period longer than the filter time constants, the output of the filter can fall below 1.1 V, causing the VCO to stop or to oscillate at its lowest frequency, $f_{off.}$ And in certain applications, the VCO output frequency must be prevented from exceeding the value corresponding to an input signal of V_{CC} – 1.1 V. In the frequency synthesizer application which follows, the active filter output is clamped, so it's useful to give some more details here, before describing the design of the synthesizer.

Clamping for a passive filter

To clamp the output of a passive filter, two additional resistors, R', are connected as shown in Fig.49. When the clamp is used in conjunction with PC2, it is recommended that the VCO centre frequency, f_0, be trimmed to near the input frequency with R2 or C1. This is because, when the loop is locked, the output of PC2 is 3-state, so the additional resistances would always bring the VCO_{IN} voltage to $0.5V_{CC}$, biasing the VCO output frequency away from the input frequency, introducing a large phase error.

The value of R' is:

$$R' = \frac{V_{CC}R3}{1.1} \tag{51}$$

where R3 is the original resistance in the filter.

At V_{CC} = 5 V,

R' = 4.545R3.

This R' alters the filter constant – R3 being replaced by the parallel combination of R3 and 0.5R'. Therefore, R3 should be increased until the combined parallel combination of R3 and 0.5R' equals the original R3. The required value of R3 (R3') is:

$$R3' = \frac{V_{CC}R3}{V_{CC} - 2.2}. \tag{52}$$

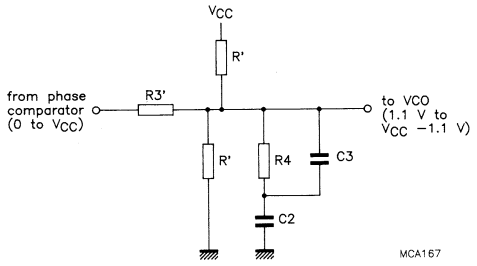


Fig.49 Output clamping for a passive filter.

Clamping for an active filter

To clamp the output of an active filter, three additional resistors, R5, R6 and R7, are connected as shown in Fig.50. This doesn't change the original filter characteristic, and the values of R5, R6 and R7 are calculated as follows.

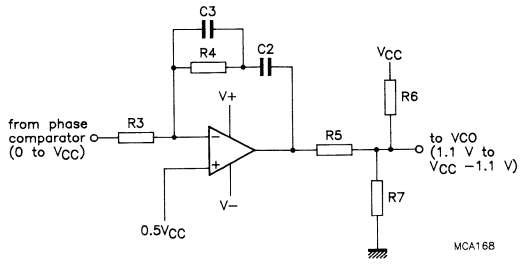


Fig.50 Output clamping for an active filter.

First, R5 is set to 10 kΩ which will lead to practical values for R6 and R7 in virtually all cases. Next, the minimum (low) and maximum (high) output voltages of the op-amp are needed (V_{high} and V_{low} respectively). These are typically 1 V above the negative supply of the op-amp and 0.5 V below the positive supply of the op-amp respectively. If it is assumed that R6 and the HCMOS PLL circuit are connected to the same supply, then:

$$R6 = \frac{R5(V_{CC} - 1.1)^2 - (1.1)^2}{1.1\{V_{high} - (V_{CC} - 1.1)\} - (V_{CC} - 1.1)(V_{low} - 1.1)} \quad (53)$$

and

$$R7 = \frac{R6R5(V_{CC} - 1.1)}{1.1R5 + \{(V_{high} - (V_{CC} - 1.1)\}R6} \quad (54)$$

Reduced loop gain

The clamping described reduces the total loop gain. For passive filters:

$$K_{new} = \frac{(V_{CC} - 2.2)}{V_{CC}} K_{old} \quad (55)$$

and for active filters:

$$K_{new} = \frac{(V_{CC} - 2.2)}{V_{high} - V_{low}} K_{old} \quad (56)$$

If the PLL design program is used, the reduced loop gain can be inserted by increasing the VCO input voltage range, which reduces the gain of the VCO, and hence of the total loop. The default VCO input voltage is calculated and displayed on the screen. For V_{CC} = 5 V, this will be 5 − 2.2 = 2.8 V. Now, if for example, $V_{high} - V_{low}$ is 28 V, the default value of 2.8 V should be multiplied by 28/2.8, yielding 28 V. The loop gain will also be altered by the same factor.

Frequency synthesizer

In this section, the design of a synthesizer using the PLL design program is described for, in turn, PC1, PC2 and PC3 first with a passive filter and then with an active filter, resulting in six designs.

If you have a copy of the PLL design program, it is a good exercise to work through this example for yourself.

The general system specifications are:

- output frequency: 2 MHz to 3 MHz
- frequency steps: 100 kHz
- settling time: <1 ms
- overshoot: <20%
- V_{CC}: 5 V

Figure 51 shows the synthesizer circuit. The external components R1 and R2 have a 1% tolerance and C1 has a 2% tolerance, resulting in a total tolerance of 24% (part-to-part spread of an HCMOS PLL circuit is 20%, see 'Part-to-part spread') to which an estimated 8% maximum temperature variation is added, making 32% in total.

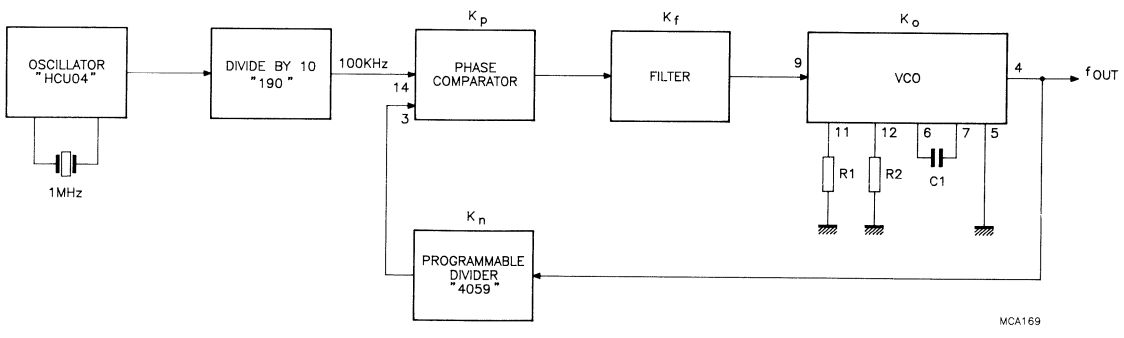


Fig.51 Frequency synthesizer.

Calculating the division ratio

The minimum and maximum programmable division ratios required are:

$$N_{min} = \frac{f_{out(min)}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20 \quad (57)$$

and

$$N_{max} = \frac{f_{out(max)}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30. \quad (58)$$

Table 3 lists the states of the control pins for a 74HC4059 programmable divide-by-N counter to step from divide-by-20 to divide-by-30, see also the PC74HC/HCT4059 data in Data Handbook IC06.

Table 3: Pin status for a 4059 programmable divider for N = 20 to 30.

N	mode 2*	J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9 to J_{16}
20	10	0	0	0	0	0	1	0	1	0
21	10 remainder 1	1	0	0	0	0	1	0	1	0
22	11	0	0	0	0	1	1	0	1	0
23	11 remainder 1	1	0	0	0	1	1	0	1	0
24	12	0	0	0	0	0	0	1	1	0
25	12 remainder 1	1	0	0	0	0	0	1	1	0
26	13	0	0	0	0	1	0	1	1	0
27	13 remainder 1	1	0	0	0	1	0	1	1	0
28	14	0	0	0	0	0	1	1	1	0
29	14 remainder 1	1	0	0	0	0	1	1	1	0
30	15	0	0	0	0	1	1	1	1	0

* selected by the mode select inputs: K_a, K_b and K_c = 1 and the latch enable: LE = 0. Mode 2 selects the first counting section of the 4059 to a divide-by-2 counter. The divide-by-N output, Q, is connected to the input of the phase comparator; V_{CC} = 5 V: GND = 0 V.

The filter components and VCO bias components are calculated by the program. The VCO centre frequency and operating range are the default values, calculated using the equations of the section 'Part-to-part spread'. This means that the external VCO components don't have to be trimmed to compensate for the VCO part-to-part spread.

The calculated results are compared with measurements on each configuration and are restricted to overshoot, settling time, pull-out range and ripple suppression, and the Bode plot. Figure 52 shows the results, as they are displayed on-screen.

The Bode plot of the open loop was measured with the injection circuit shown in Appendix C together with an HP3577A network analyser.

INPUT PARAMETERS

PC	: 1	fin	(Hz) :	1.000E+05	Spread input freq.	(%) :	0.0
N	: 30.0	2fR	(Hz) :	2.897E+06	Part-to-part spread	(%) :	32.0
Filter :	1	f0	(Hz) :	2.963E+06	Vcc	(Volt) :	5.0

VCO and FILTER PARAMETERS

T1 (sec) :	1.6E-02	T2 (sec) :	3.0E-04	T3 (sec) :	2.5E-05
f1 (Hz) :	9.8E+00	f2 (Hz) :	5.3E+02	f3 (Hz) :	6.3E+03
R1 (Ohm) :	1.5E+04	R3 (Ohm) :	4.4E+02	R4 (Ohm) :	8.4E+00
R2 (Ohm) :	1.3E+05	C2 (Far) :	3.6E-05	C3 (Far) :	3.0E-06
C1 (Far) :	1.0E-10				

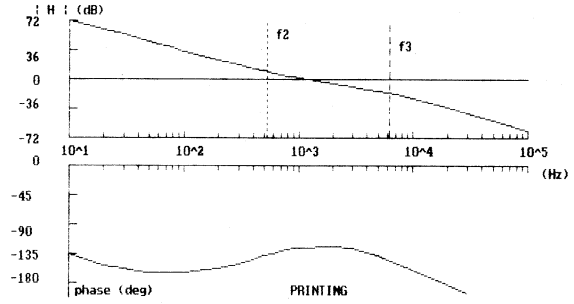
DYNAMIC PARAMETERS

Wn/2π	(Hz) : 7.3E+02	pull-in time	(sec) :	3.3E-02	
W_0dB/2π	(Hz) : 1.3E+03	pull-in range	(Hz) :	1.2E+04	
zeta	: 0.70	pull-out range	(Hz) :	2.2E+03	
overshoot	(%) : 21.03	hold range	(Hz) :	8.6E+04	
Kv	: 3.4E+05	settling time (<5%)	(sec) :	1.0E-03	
Winput/W_0dB	: 79.6	lock-in range	(Hz) :	1.6E+03	
phasemargin with C3 (deg)	: 57	ripple suppr. with C3	(dB) :	-46	
without C3 (deg)	: 67	without C3	(dB) :	-16	
zetamin	: 0.70	Wnmin/2π	(Hz) :	7.3E+02	
zetamax	: 0.86	Wnmax/2π	(Hz) :	9.0E+02	

Philips Components

Optimize ? (Y/N): Y

(a)



(b)

Fig.52 (a) Original loop parameters and (b) calculated Bode plot for a PLL using PC1 and a passive filter.

INPUT PARAMETERS

PC	: 1	fin	(Hz) :	1.000E+05	Spread input freq.	(%) :	0.0
N	: 30.0	2fR	(Hz) :	2.897E+06	Part-to-part spread	(%) :	32.0
Filter :	1	f0	(Hz) :	2.963E+06	Vcc	(Volt) :	5.0

VCO and FILTER PARAMETERS

T1 (sec) :	1.2E-03	T2 (sec) :	8.2E-05	T3 (sec) :	7.2E-06
f1 (Hz) :	1.2E+02	f2 (Hz) :	1.9E+03	f3 (Hz) :	2.2E+04
R1 (Ohm) :	1.5E+04	R3 (Ohm) :	4.4E+02	R4 (Ohm) :	3.0E+01
R2 (Ohm) :	1.3E+05	C2 (Far) :	2.7E-06	C3 (Far) :	2.4E-07
C1 (Far) :	1.0E-10				

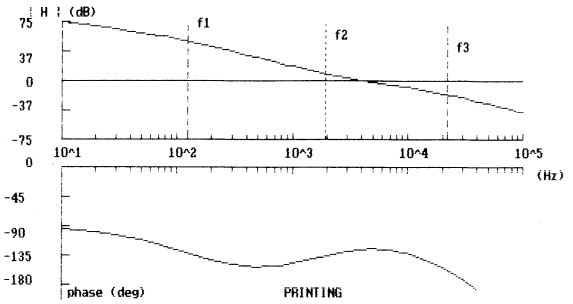
DYNAMIC PARAMETERS

Wn/2π	(Hz) : 2.6E+03	pull-in time	(sec) :	2.6E-03	
W_0dB/2π	(Hz) : 4.4E+03	pull-in range	(Hz) :	2.2E+04	
zeta	: 0.70	pull-out range	(Hz) :	8.0E+03	
overshoot	(%) : 21.03	hold range	(Hz) :	8.6E+04	
Kv	: 3.4E+05	settling time (<5%)	(sec) :	2.8E-04	
Winput/W_0dB	: 22.7	lock-in range	(Hz) :	5.7E+03	
phasemargin with C3 (deg)	: 55	ripple suppr. with C3	(dB) :	-23	
without C3 (deg)	: 64	without C3	(dB) :	-6	
zetamin	: 0.70	Wnmin/2π	(Hz) :	2.6E+03	
zetamax	: 0.86	Wnmax/2π	(Hz) :	3.2E+03	

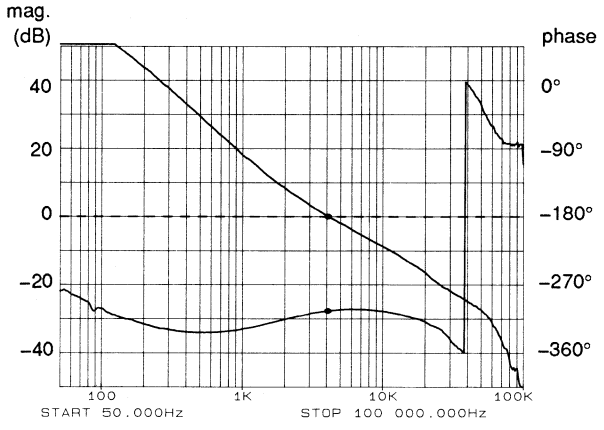
Philips Components

Optimize ? (Y/N): Y

(a)



(b)



(c)

Fig.53 (a) Modified loop parameters and (b) calculated Bode plot for a PLL using PC1 and a passive filter. (c) measured Bode plot; phase margin is 55.9° at 4.120 kHz (0 dB).

Designing with the program

During the calculation of the PLL parameters, the following error message is displayed: "Error, switching between channels will cause the loop to lose lock. Increase pull-out range to 5.1 kHz."
For example, if the divider in the feedback switches from 21 to 20, the frequency step on the phase comparator input is:

$$100\ \text{kHz} - \frac{2.1\ \text{MHz}}{20} = 5\ \text{kHz}.$$

Unless the pull-out range exceeds this frequency step, the loop will lose lock when the divider switches, taking the pull-in time to regain lock. In this example, the pull-out range was set to 8 kHz via option 9 of the optimization menu for extra margin. The new results and Bode plot are shown in Fig.53.

In all calculations, the program uses the maximum division ratio, N_{max}, because this gives worst-case values for overshoot, ζ, and settling time. With 'option 0', all parameters and the Bode plot can be checked by changing N from N_{max} to N_{min}.

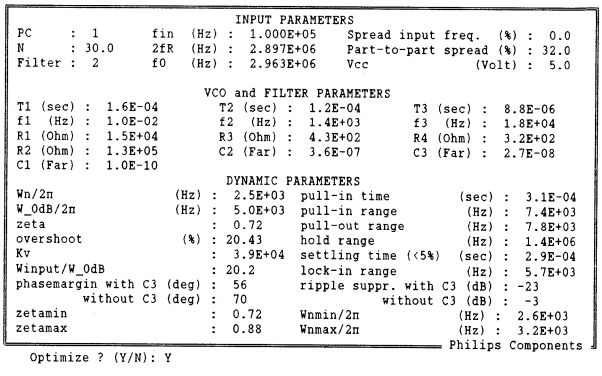
The results for the remaining five designs are given in Figs 54 to 58. In the case of PC2 used with a passive filter, the gain variation of PC2 is taken into account. In the case of PC3 with a passive filter, the same error message was displayed as for the example with PC1 just described, and here too the pull-out range was increased to 8 kHz.

Figure 59 shows the overshoot of a real synthesizer while switching from a division ratio of 28 to 29 and from 20 to 21. The lower-gain loops using PC1 and PC3 with a passive filter have less overshoot than that calculated by the program. This is because the program uses only the step response for a high-gain loop (Fig.41), whereas in practice the loop changes gradually from a high-gain loop to a low-gain loop (Fig.40). In all cases, the measured overshoot was close to that calculated (21%) as was settling time.

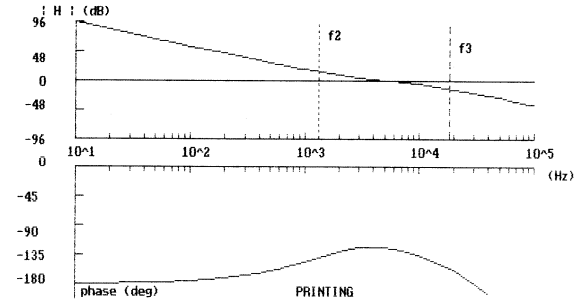
To check the need to optimize loops using PC1 owing to the small pull-out range, a synthesizer was built according to the non-optimized parameters. The synthesizer would not work and would not lock at all at division ratios away from the centre ratio of 25.

The ripple suppression ratio is only a rough approximation, so the measured values can be expected to differ from those calculated especially when the calculated value is less than about −10 dB. This is because the modulation index is now large and the first-order approach is no longer accurate. However, the values calculated by the program are useful to see improvements during optimization, and if the ripple suppression rises above −10 dB, exact values are usually not of interest because the instability of the VCO output signal is often unacceptable. Figure 60 shows the ripple suppression (measured on the VCO output signal). The ripple suppression can be improved by using the optimize facility, but this will increase the settling time.

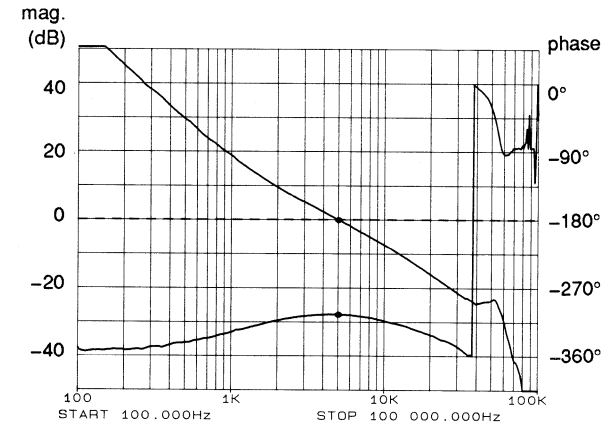
Note, these design examples are only intended to illustrate how the program operates. the values presented are NOT the optimum that can be achieved with the 74HC/HCT4046A. In practice, the PLLs would be optimized further than shown in the examples to improve performance, for example, the ripple suppression.



(a)

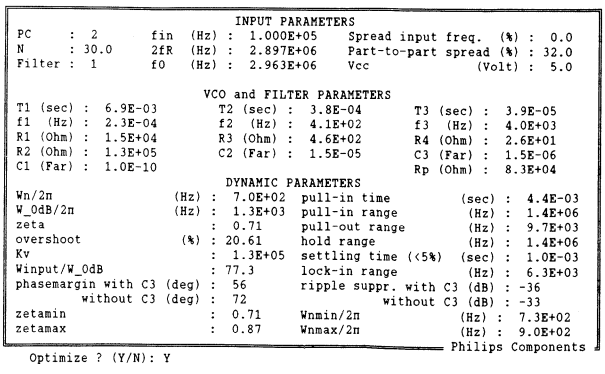


(b)

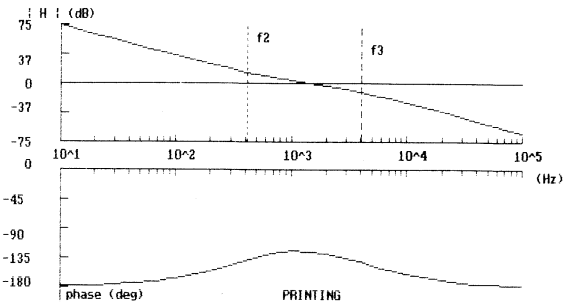


(c)

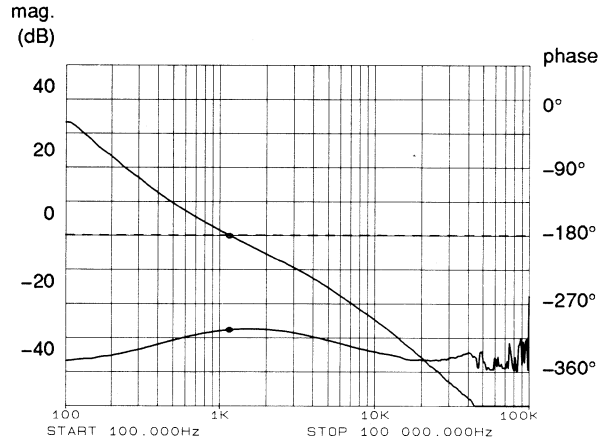
Fig.54 (a) Loop parameters and (b) calculated Bode plot for a PLL using PC1 with an active filter. (c) measured Bode plot; phase margin is 54.9° at 5.056 kHz (0 dB).



(a)



(b)



(c)

Fig.55 (a) Loop parameters and (b) calculated Bode plot for a PLL using PC2 with a passive filter. (c) measured Bode plot; phase margin is 55.5° at 1.164 kHz (0 dB).

INPUT PARAMETERS

PC	: 2	fin	(Hz) : 1.000E+05	Spread input freq.	(%) : 0.0		
N	: 30.0	2fR	(Hz) : 2.897E+06	Part-to-part spread	(%) : 32.0		
Filter	: 2	f0	(Hz) : 2.963E+06	Vcc	(Volt) : 5.0		

VCO and FILTER PARAMETERS

T1 (sec)	: 5.0E-04	T2 (sec)	: 3.8E-04	T3 (sec)	: 3.9E-05
f1 (Hz)	: 3.2E-03	f2 (Hz)	: 4.1E+02	f3 (Hz)	: 4.0E+03
R1 (Ohm)	: 1.5E+04	R3 (Ohm)	: 4.5E+02	R4 (Ohm)	: 3.5E+02
R2 (Ohm)	: 1.3E+05	C2 (Far)	: 1.1E-06	C3 (Far)	: 1.1E-07
C1 (Far)	: 1.0E-10			Rp (Ohm)	: 8.3E+04

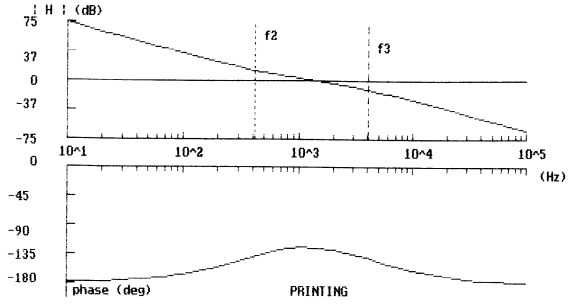
DYNAMIC PARAMETERS

Wn/2π	(Hz) : 7.0E+02	pull-in time	(sec) : 3.0E-03		
W_0dB/2π	(Hz) : 1.3E+03	pull-in range	(Hz) : 1.4E+06		
zeta	: 0.71	pull-out range	(Hz) : 9.7E+03		
overshoot	(%) : 20.61	hold range	(Hz) : 1.4E+06		
Kv	: 9.7E+03	settling time (<5%)	(sec) : 1.0E-03		
Winput/W_0dB	: 77.3	lock-in range	(Hz) : 6.3E+03		
phasemargin with C3	(deg) : 56	ripple suppr. with C3	(dB) : -32		
without C3	(deg) : 72	without C3	(dB) : -29		
zetamin	: 0.71	Wnmin/2π	(Hz) : 7.3E+02		
zetamax	: 0.87	Wnmax/2π	(Hz) : 9.0E+02		

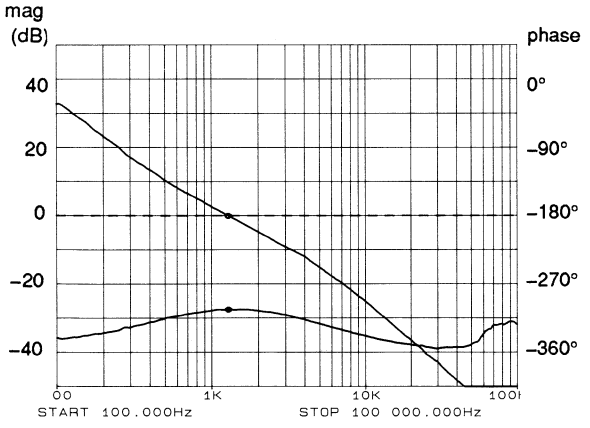
Philips Components

Optimize ? (Y/N): Y

(a)



(b)



(c)

Fig.56 (a) Loop parameters and (b) calculated Bode plot for a PLL using PC2 with an active filter. (c) measured Bode plot; phase margin is 56.7° at 1.291 kHz (0 dB).

INPUT PARAMETERS

PC	: 3	fin	(Hz) : 1.000E+05	Spread input freq.	(%) : 0.0		
N	: 30.0	2fR	(Hz) : 2.897E+06	Part-to-part spread	(%) : 32.0		
Filter	: 1	f0	(Hz) : 2.963E+06	Vcc	(Volt) : 5.0		

VCO and FILTER PARAMETERS

T1 (sec)	: 3.0E-03	T2 (sec)	: 1.9E-04	T3 (sec)	: 1.6E-05
f1 (Hz)	: 5.0E+01	f2 (Hz)	: 8.6E+02	f3 (Hz)	: 9.9E+03
R1 (Ohm)	: 1.5E+04	R3 (Ohm)	: 4.4E+02	R4 (Ohm)	: 2.7E+01
R2 (Ohm)	: 1.3E+05	C2 (Far)	: 6.8E-06	C3 (Far)	: 5.9E-07
C1 (Far)	: 1.0E-10				

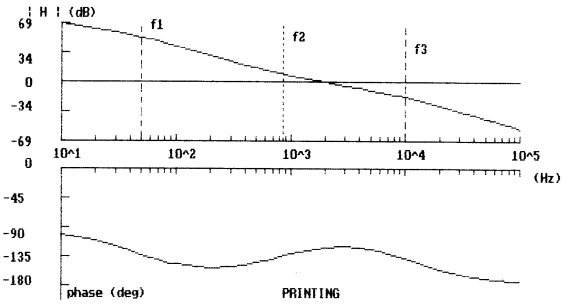
DYNAMIC PARAMETERS

Wn/2π	(Hz) : 1.2E+03	pull-in time	(sec) : 6.4E-03		
W_0dB/2π	(Hz) : 2.0E+03	pull-in range	(Hz) : 2.1E+04		
zeta	: 0.70	pull-out range	(Hz) : 8.0E+03		
overshoot	(%) : 21.03	hold range	(Hz) : 8.6E+04		
Kv	: 1.7E+05	settling time (<5%)	(sec) : 6.3E-04		
Winput/W_0dB	: 50.6	lock-in range	(Hz) : 5.1E+03		
phasemargin with C3	(deg) : 59	ripple suppr. with C3	(dB) : -19		
without C3	(deg) : 68	without C3	(dB) : -0		
zetamin	: 0.70	Wnmin/2π	(Hz) : 1.2E+03		
zetamax	: 0.86	Wnmax/2π	(Hz) : 1.4E+03		

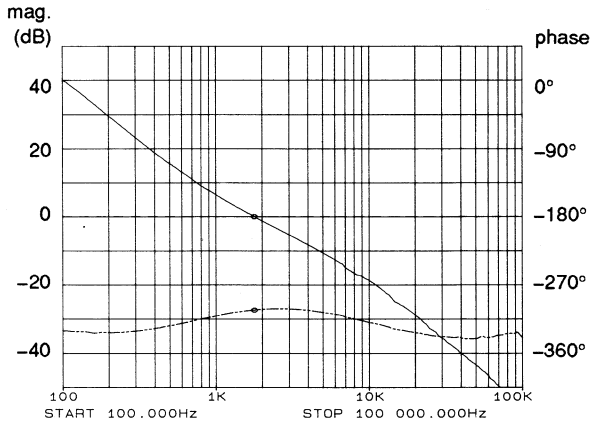
Philips Components

Optimize ? (Y/N): Y

(a)



(b)

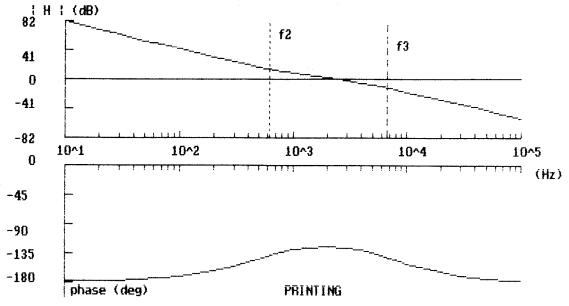


(c)

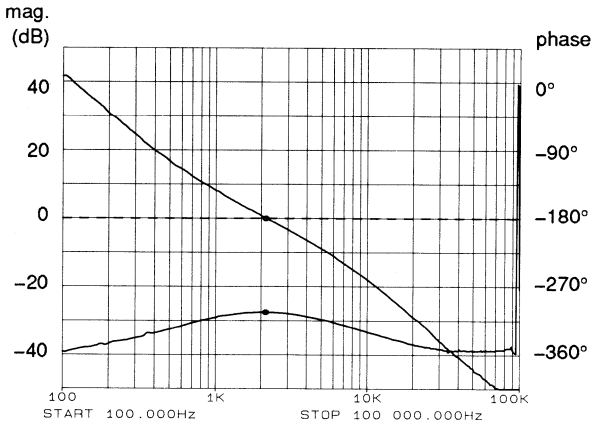
Fig.57 (a) Loop parameters and (b) calculated Bode plot for a PLL using PC3 with a passive filter. (c) measured Bode plot; phase margin is 57.4° at 1.785 kHz (0 dB).

```
                        INPUT PARAMETERS
PC      :  3        fin  (Hz) :  1.000E+05    Spread input freq.  (%) :  0.0
N       : 30.0      2fR  (Hz) :  2.897E+06    Part-to-part spread (%) : 32.0
Filter :  2         f0   (Hz) :  2.963E+06    Vcc                (Volt) :  5.0

                     VCO and FILTER PARAMETERS
T1 (sec) :  4.0E-04          T2 (sec) :  2.4E-04        T3 (sec) :  2.4E-05
f1  (Hz) :  4.0E-03          f2  (Hz) :  6.5E+02        f3  (Hz) :  6.5E+03
R1 (Ohm) :  1.5E+04          R3 (Ohm) :  4.4E+02        R4 (Ohm) :  2.7E+02
R2 (Ohm) :  1.3E+05          C2 (Far) :  9.1E-07        C3 (Far) :  9.1E-08
C1 (Far) :  1.0E-10

                      DYNAMIC PARAMETERS
Wn/2π                (Hz) :  1.1E+03  pull-in time          (sec) :  8.0E-04
W_0dB/2π             (Hz) :  2.1E+03  pull-in range          (Hz) :  7.0E+03
zeta                      :  0.72     pull-out range         (Hz) :  7.7E+03
overshoot             (%) : 20.25     hold range             (Hz) :  1.4E+06
Kv                        :  1.9E+04  settling time (<5%)   (sec) :  6.5E-04
Winput/W_0dB              : 48.6      lock-in range          (Hz) :  5.0E+03
phasemargin with C3 (deg) :  56       ripple suppr. with C3 (dB) : -22
         without C3 (deg) :  72                  without C3 (dB) :   1
zetamin                   :  0.72     Wnmin/2π               (Hz) :  1.1E+03
zetamax                   :  0.89     Wnmax/2π               (Hz) :  1.4E+03
                                                    Philips Components

Optimize ? (Y/N): Y
```

(a)

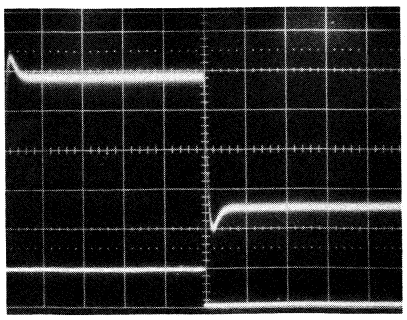


(b)

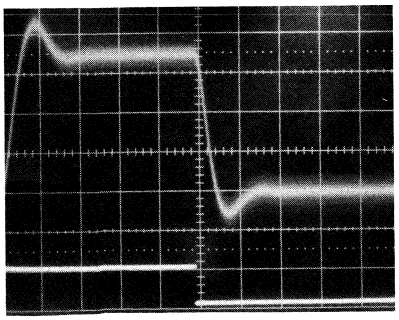


(c)

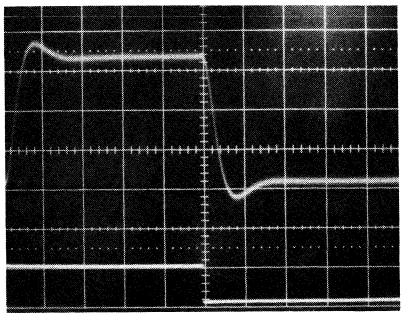
Fig.58 (a) Loop parameters and (b) calculated Bode plot for a PLL using PC3 with an active filter. (c) measured Bode plot; phase margin is 56.0° at 2.160 kHz (0 dB).



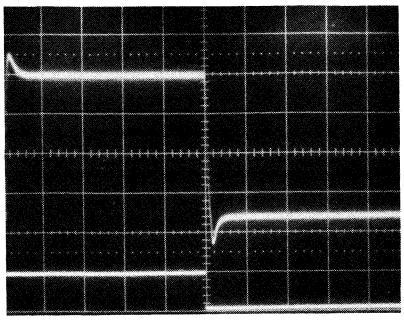
(a) with passive filter; N1 = 28/29;
low-gain loop; 15% overshoot.



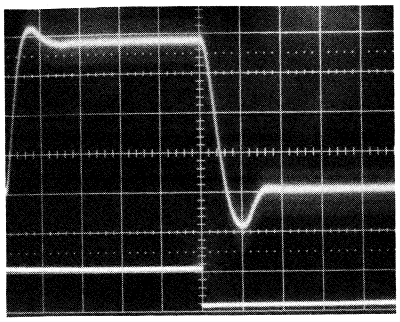
(e) with passive filter; N1 = 28/29;
21% overshoot.



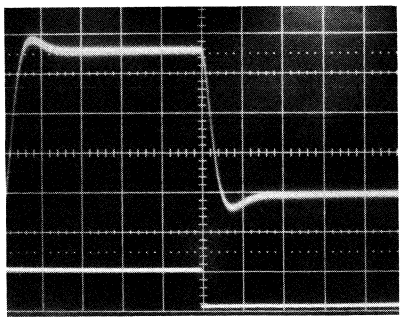
(i) with passive filter; N1 = 28/29;
18% overshoot.



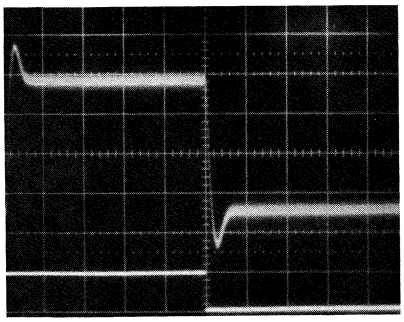
(b) with passive filter; N1 = 20/21;
low-gain loop; 15% overshoot.



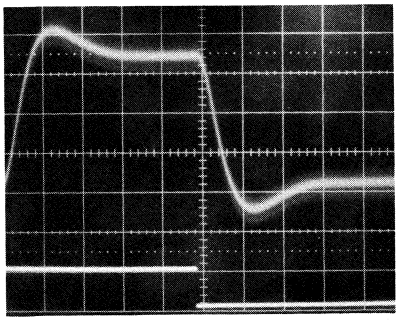
(f) with passive filter; N1 = 20/21;
23% overshoot.



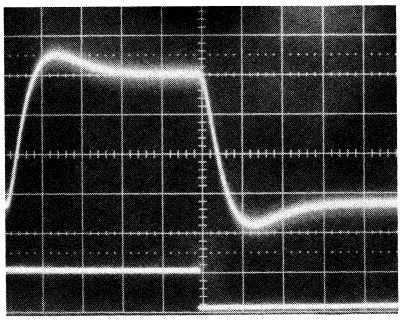
(j) with passive filter; N1 = 20/21;
low-gain loop; 14% overshoot.



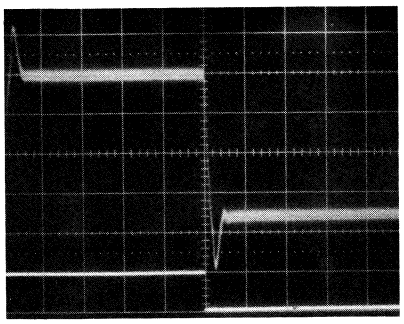
(c) with active filter; N1 = 28/29;
22% overshoot.



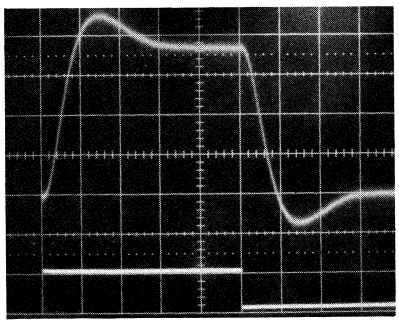
(g) with active filter; N1 = 28/29;
21% overshoot.



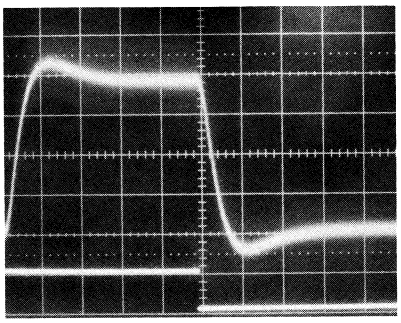
(k) with active filter; N1 = 28/29;
20% overshoot.



(d) with active filter; N1 = 20/21.
28% overshoot.



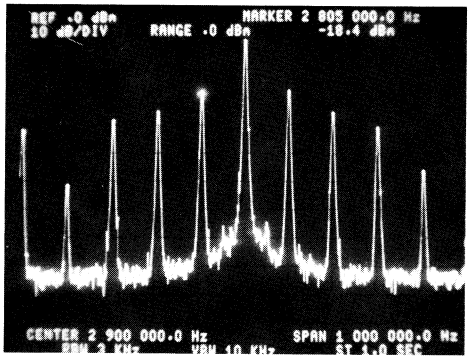
(h) with active filter; N1 = 20/21;
21% overshoot.



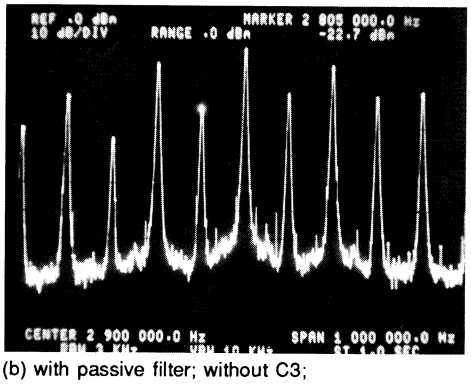
(l) with active filter; N1 = 20/21;
19% overshoot.

PC1. PC2. PC3.

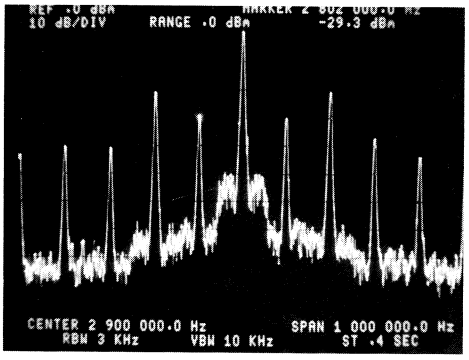
Fig.59 Overshoot and settling time for the frequency synthesizer. Hor. scale: 0.5 ms/div.



(a) with passive filter; with C3;



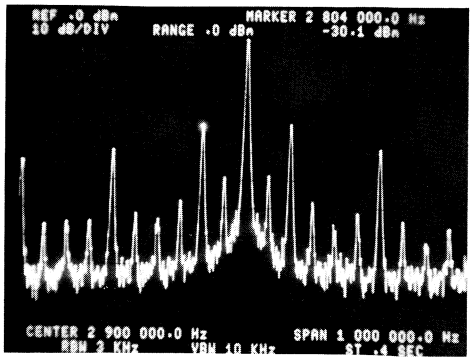
(b) with passive filter; without C3;



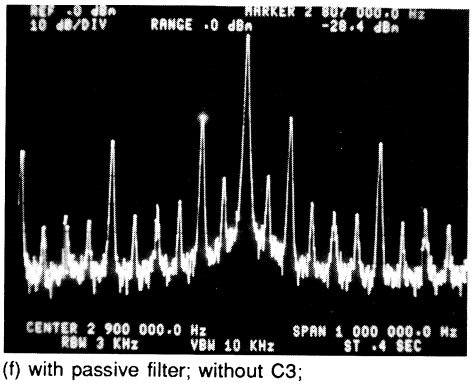
(c) with active filter; with C3;

loop unable
to acquire lock

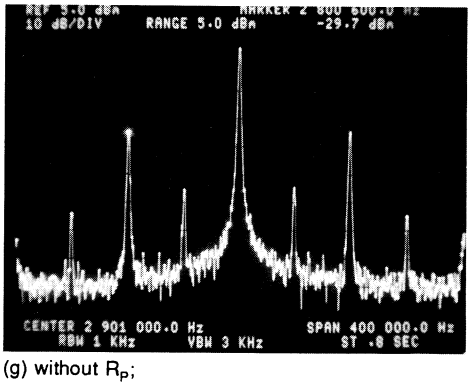
(d) with active filter; without C3.



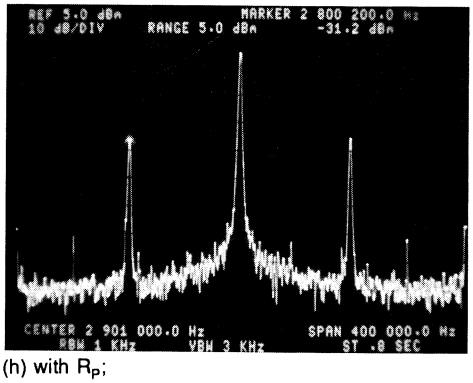
(e) with passive filter; with C3;



(f) with passive filter; without C3;



(g) without R_P;

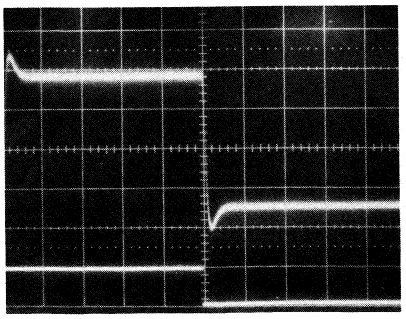


(h) with R_P;

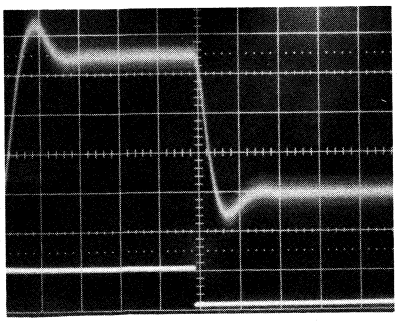
PC1.

PC2.

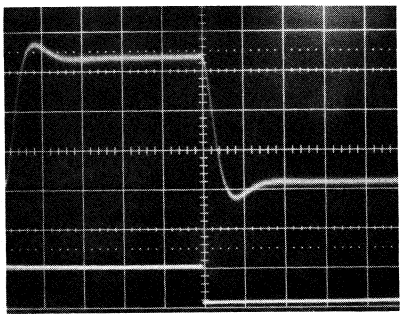
Fig.60 Ripple suppression. Vert. scale: 10 dB/div. Hor. scale 100 kHz/div.



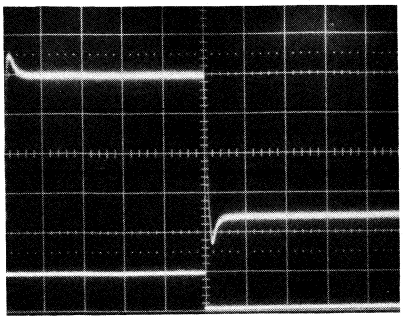
(a) with passive filter; N1 = 28/29;
low-gain loop; 15% overshoot.



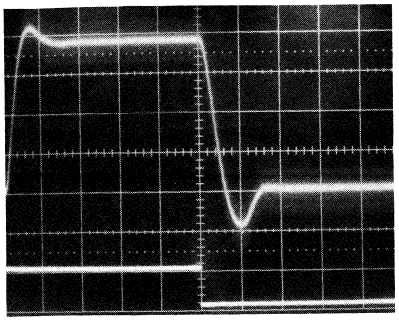
(e) with passive filter; N1 = 28/29;
21% overshoot.



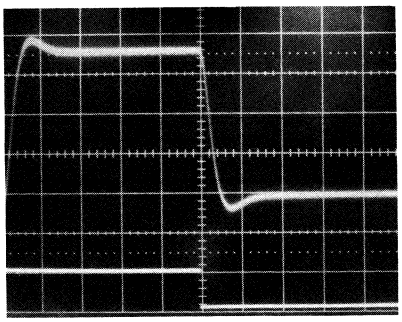
(i) with passive filter; N1 = 28/29;
18% overshoot.



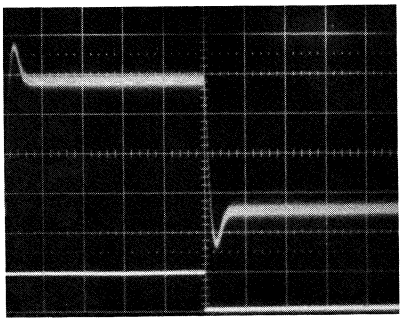
(b) with passive filter; N1 = 20/21;
low-gain loop; 15% overshoot.



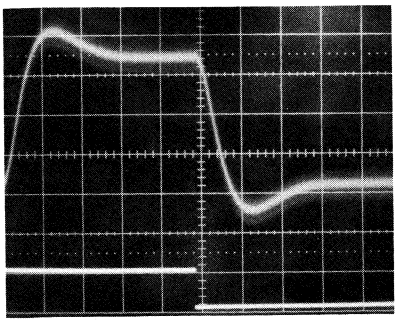
(f) with passive filter; N1 = 20/21;
23% overshoot.



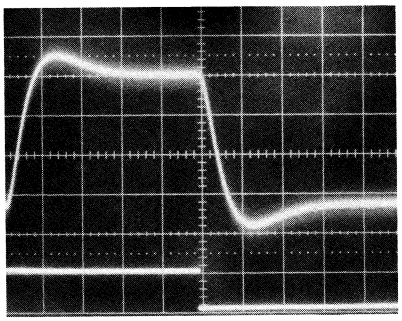
(j) with passive filter; N1 = 20/21;
low-gain loop; 14% overshoot.



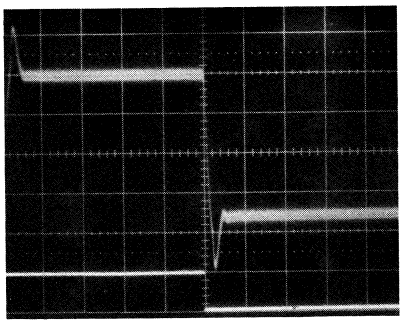
(c) with active filter; N1 = 28/29;
22% overshoot.



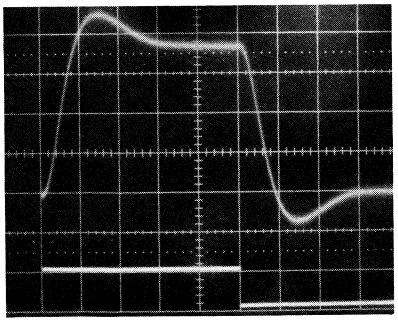
(g) with active filter; N1 = 28/29;
21% overshoot.



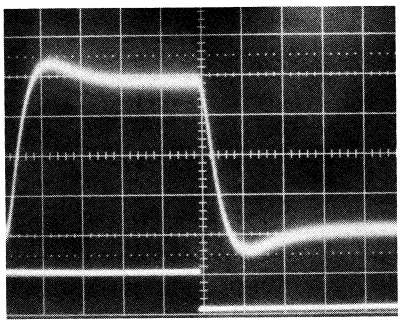
(k) with active filter; N1 = 28/29;
20% overshoot.



(d) with active filter; N1 = 20/21.
28% overshoot.



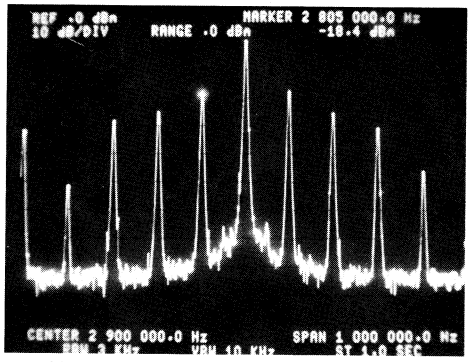
(h) with active filter; N1 = 20/21;
21% overshoot.



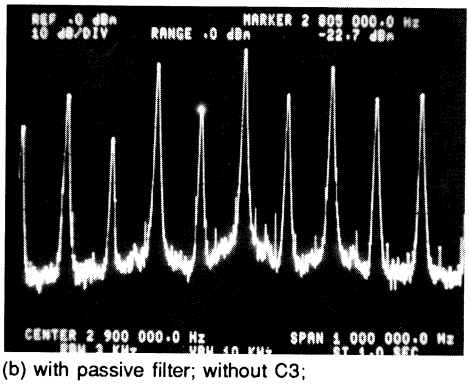
(l) with active filter; N1 = 20/21;
19% overshoot.

PC1. PC2. PC3.

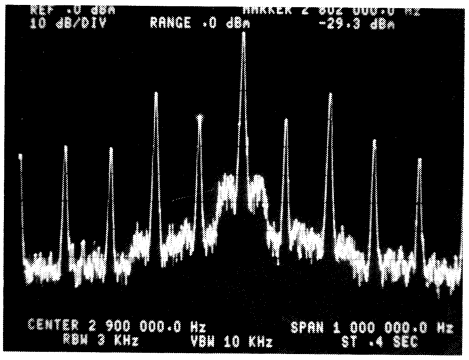
Fig.59 Overshoot and settling time for the frequency synthesizer. Hor. scale: 0.5 ms/div.



(a) with passive filter; with C3;



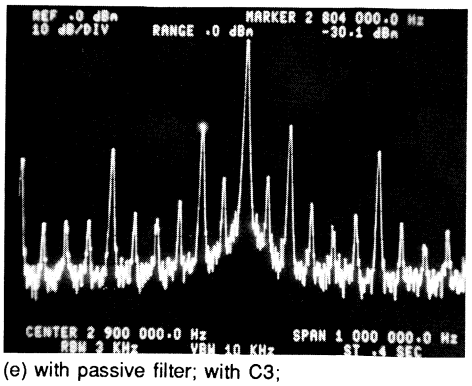
(b) with passive filter; without C3;



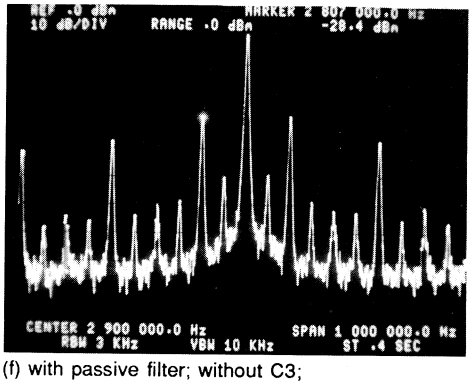
(c) with active filter; with C3;

loop unable
to acquire lock

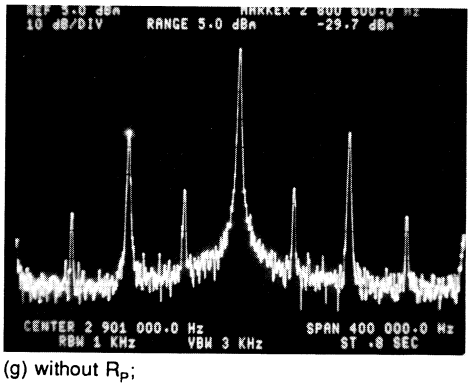
(d) with active filter; without C3.



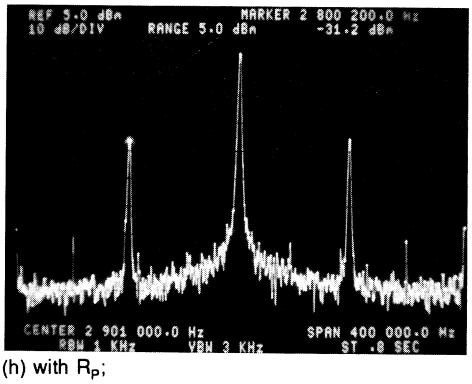
(e) with passive filter; with C3;



(f) with passive filter; without C3;



(g) without R_P;

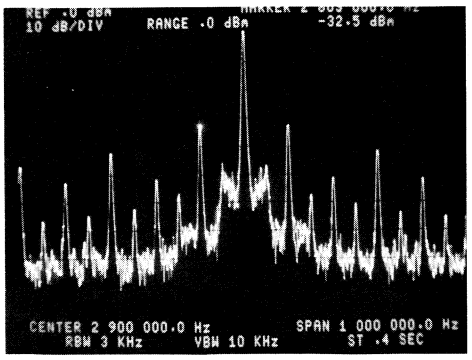


(h) with R_P;

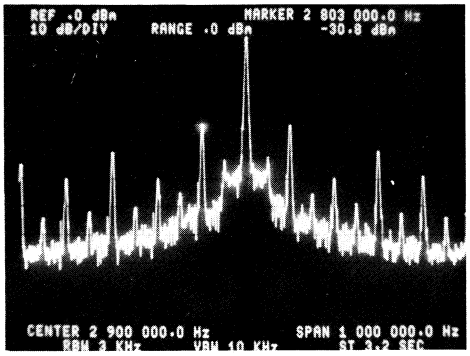
PC1.

PC2.

Fig.60 Ripple suppression. Vert. scale: 10 dB/div. Hor. scale 100 kHz/div.

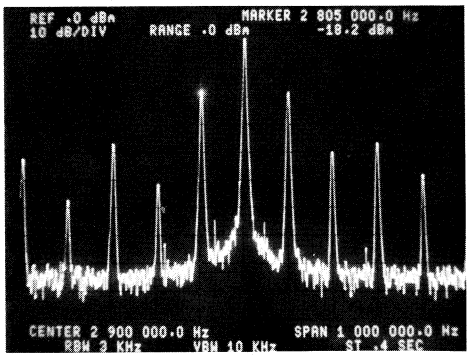


(i) with active filter; with C3;

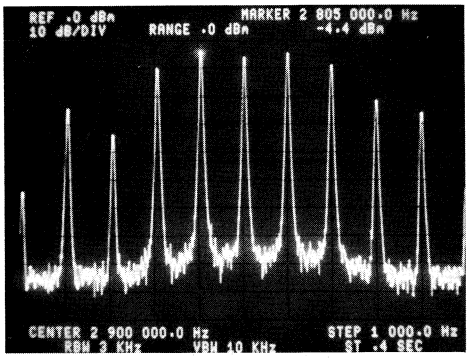


(j) with active filter; without C3.

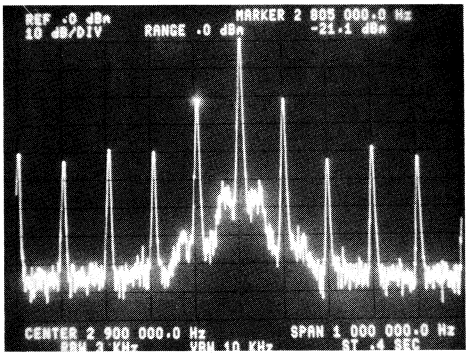
PC2 cont.



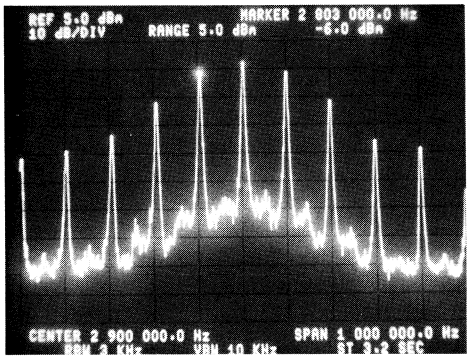
(k) with passive filter; with C3;



(l) with passive filter; without C3;



(m) with active filter; with C3;



(n) with active filter; with C3 = 10 nF.
With C3 < 10 nF, the loop was unable to acquire lock.

PC3.

Video monitor line synchronizer

Figure 61 shows the circuit schematic of a video monitor line synchronizer designed with the help of the PLL design program. The synchronizer has the following features:

- can be synchronized over at least one octave (double frequency monitor);
- produces no visible phase jitter;
- slew rate clamping to protect the drivers in the horizontal deflection stage from very fast frequency changes;
- equal lock and hold ranges;
- fast settling time after a frequency change.

In this synchronizer, a non-composite sync signal is used to limit the circuitry needed; the circuitry required if a composite signal is used is not described because it is the subject of a patent pending.

The input signal (horizontal sync) which can range from 15.625 kHz to 31.250 kHz is entered in the design program as an f_{in} of 23.4375 kHz with an expected deviation of 35%.

Phase comparator PC2 is used because it has the best lock and hold range of the three phase comparators, as well as edge-triggered detection and, here, a noise-free input signal.

An active loop filter was chosen because the input frequency range is so large that with a passive filter, the phase comparator gain would vary too much. In addition, it is easy to insert a slew rate clamp in an active filter. In Fig.61, the clamp is simply the two back-to-back zener diodes and series capacitance of 470 nF. The 360 kΩ resistor (R_p) connected to the output of PC2 reduces phase jitter to an imperceptible level. The filter output is clamped and the component values were selected using Eqs.(45) to (50) and V_{low} = 1 V, V_{high} = 25.5 V (the op-amp supply is 26 V). The output clamping lowers the loop gain and this is entered in the PLL design program by changing the VCO input voltage range from the default value of 2.8 V to (24.4/2.8)2.8 = 24.4 V.

The positive input of the op-amp is biased at $0.5V_{CC}$ = 2.5 V. Note, because the op-amp inverts the output from the phase comparator, the horizontal sync input is connected to the $COMP_{IN}$ input instead of the SIG_{IN} input. The tolerance of the external components for the VCO (1% for R1 and R2; 2% for C1) result in a VCO spread of 24%. When an 8% spread is added for temperature changes up to 85 °C, the total spread is 32%. The program calculates the centre frequency f_0 and the VCO operating range $2f_R$ such that trimming is not required. After a warning message, ω_n was lowered to 650 Hz via the optimization facility.

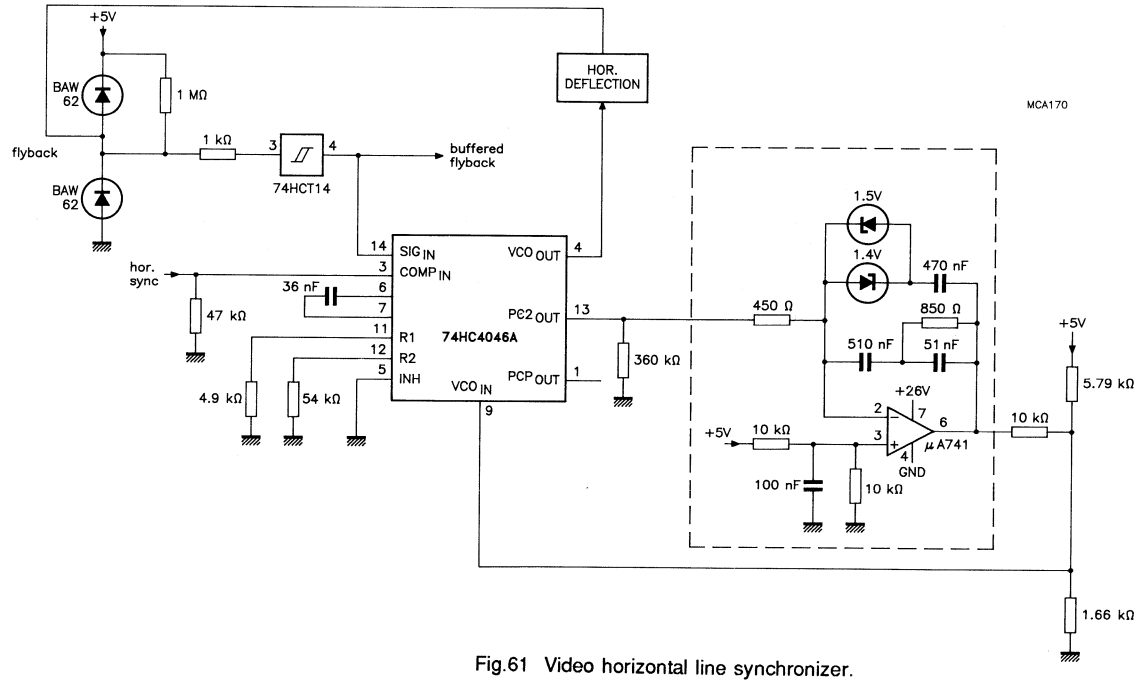
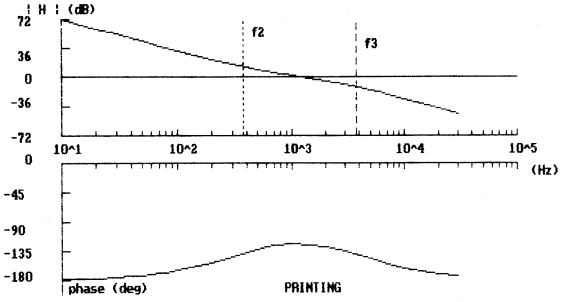


Fig.61 Video horizontal line synchronizer.

Figure 62(a) shows the results of the calculation program. With a settling time of 0.26 ms and $\zeta = 0.72$, no further optimization appears necessary as the Bode plot (Fig.62(b)) and Fig.63 confirms.

```
                              INPUT PARAMETERS
PC      :  2        fin  (Hz) :  2.344E+04    Spread input freq.  (%) : 35.0
N       :  1.0      2fR  (Hz) :  3.499E+04    Part-to-part spread (%) : 32.0
Filter  :  2        f0   (Hz) :  2.904E+04    Vcc                (Volt) :  5.0

                          VCO and FILTER PARAMETERS
T1 (sec) :  2.3E-04          T2 (sec) :  4.4E-04        T3 (sec) :  4.3E-05
f1  (Hz) :  7.0E-03          f2  (Hz) :  3.7E+02        f3  (Hz) :  3.7E+03
R1 (Ohm) :  4.9E+03          R3 (Ohm) :  4.5E+02        R4 (Ohm) :  8.5E+02
R2 (Ohm) :  5.4E+04          C2 (Far) :  5.1E-07        C3 (Far) :  5.1E-08
C1 (Far) :  3.6E-08                                     Rp (Ohm) :  3.6E+05
                          DYNAMIC PARAMETERS
Wn/2n                  (Hz) :  6.2E+02  pull-in time          (sec) :  1.2E-03
W_0dB/2n               (Hz) :  1.2E+03  pull-in range          (Hz) :  1.7E+04
zeta                        :  0.72     pull-out range         (Hz) :  8.7E+03
overshoot               (%) : 20.25     hold range             (Hz) :  1.7E+04
Kv                          :  3.5E+03  settling time         (sec) :  2.6E-04
Winput/W_0dB                : 20.3      lock-in range          (Hz) :  5.7E+03
phasemargin with C3 (deg) :  56         ripple suppr. with C3 (dB) : -59
        without C3 (deg) :  72                    without C3 (dB) : -59
W-3dB/2n closed loop (Hz) :  1.3E+03

                                                        Philips Components
Optimize ? (Y/N): Y
```

(a)



(b)

Fig.62 (a) Loop parameters and (b) Bode plot of the video horizontal line synchronizer generated by the design program. The Bode plot of the real circuit (see Fig.63) is extremely close to the plot generated by the program.

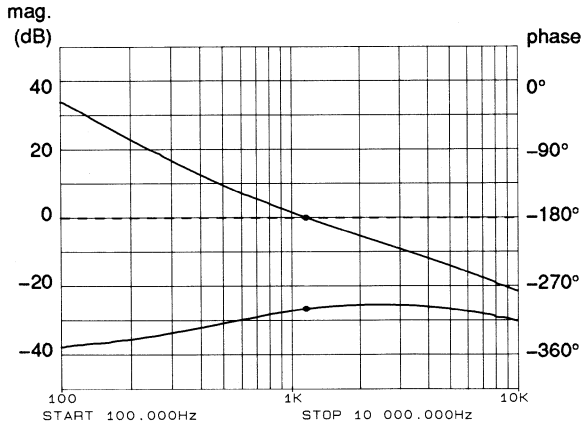


Fig.63 Bode plot for the video horizontal line synchronizer built using the design program. The phase margin is 60.5° at 1.163 kHz (0 dB).

FM demodulator

Figure 64 is a modulation tracking loop, or FM demodulator designed with the help of the design program. The centre frequency is 10.7 MHz which is very close to the maximum specified in the data sheet at V_{CC} = 4.5 V, making it a worst-case situation for the 74HC/HCT4046A for demodulation. Phase comparator PC1 was chosen because it is expected that the input signal will be noisy. However, owing to the limited capture and hold range of this phase comparator, R2 is made adjustable. A passive filter was chosen because the loop delay must be kept to a minimum and the phase difference between the input signal and the VCO frequency may differ from 90°.

For the program, a ±75 kHz peak frequency deviation is used and a 1 kHz modulation frequency. Since R2 is adjustable, the VCO part-to-part spread is set to zero.

Figure 65(a) shows the results from running the design program once. The pull-out range was set to a safe value of 310 kHz and capacitor C3 which, at these high frequencies, affects the output transitions of PC1 significantly, was removed. The optimized parameters and the Bode plot are shown in Fig.66.

The demodulated output at the DEM_{OUT} pin is connected to a de-emphasis circuit. The distortion is typically 0.5% but depends on the value of R2. The signal-to-noise ratio is about 55 dB. Both values are good for a standard general-purpose PLL circuit and they improve considerably at lower centre frequencies.

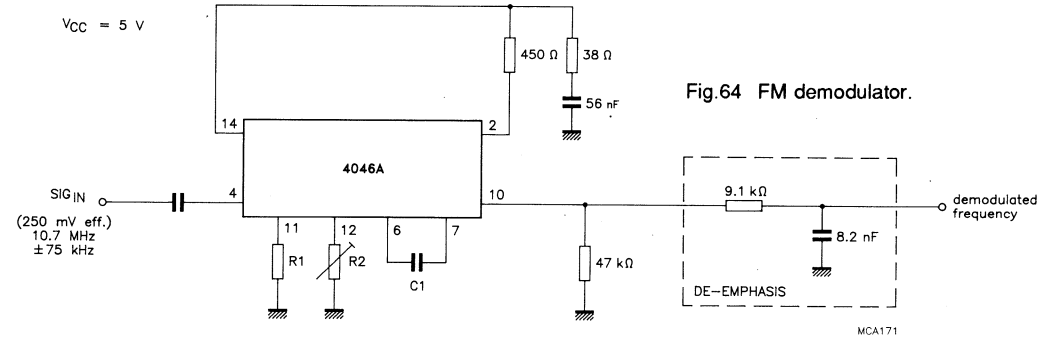
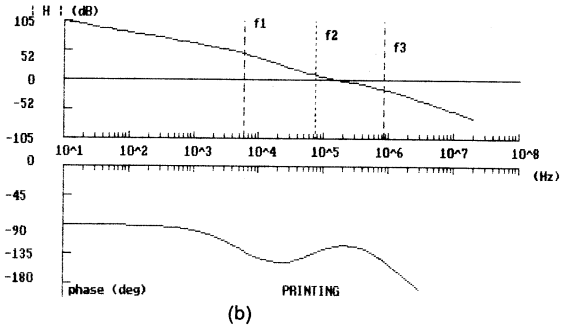


Fig.64 FM demodulator.

```
                    INPUT PARAMETERS
PC      :  1        fin  (Hz) :  1.070E+07    Spread input freq.  (%) :  0.0
N       :  1.0      2fR  (Hz) :  3.000E+06    Part-to-part spread (%) :  0.0
Filter  :  1        f0   (Hz) :  1.070E+07    Vcc               (Volt) :  5.0

                  VCO and FILTER PARAMETERS
T1 (sec)  :  2.5E-05        T2 (sec)  :  2.1E-06        T3 (sec)  :  1.9E-07
f1  (Hz)  :  5.9E+03        f2  (Hz)  :  7.5E+04        f3  (Hz)  :  8.4E+05
R1 (Ohm)  :  1.3E+04        R3 (Ohm)  :  4.5E+02        R4 (Ohm)  :  3.8E+01
R2 (Ohm)  :  7.6E+03        C2 (Far)  :  5.6E-08        C3 (Far)  :  5.0E-09
C1 (Far)  :  1.0E-10

                    DYNAMIC PARAMETERS
Wn/2π                  (Hz)  :  1.0E+05  pull-in time          (sec)  :  5.4E-05
W_0dB/2π               (Hz)  :  1.7E+05  pull-in range         (Hz)  :  7.7E+05
zeta                         :  0.70     pull-out range       (Hz)  :  3.1E+05
overshoot               (%)  : 21.03     hold range           (Hz)  :  1.5E+06
Kv                           :  1.1E+07  settling time        (sec)  :  1.8E-06
Winput/W_0dB                 : 63.7      lock-in range        (Hz)  :  2.2E+05
phasemargin with C3  (deg)   :  58       ripple suppr. with C3 (dB) : -71
      without C3     (deg)   :  67                 without C3 (dB) : -44
W-3dB/2π closed loop (Hz)    :  2.0E+05
peak phase error     (deg)   :  4.3E-01
                                                    Philips Components
Optimize ? (Y/N): Y
```

(a)

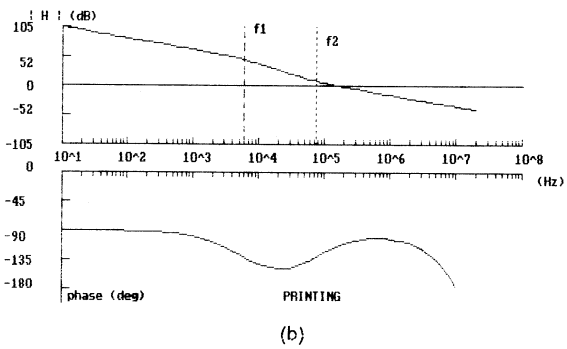


(b)

Fig.65 (a)Loop parameters and (b) Bode plot of the FM demodulator after running the program once.

```
                    INPUT PARAMETERS
PC      :  1        fin  (Hz) :  1.070E+07    Spread input freq.  (%) :  0.0
N       :  1.0      2fR  (Hz) :  3.000E+06    Part-to-part spread (%) :  0.0
Filter  :  1        f0   (Hz) :  1.070E+07    Vcc               (Volt) :  5.0

                  VCO and FILTER PARAMETERS
T1 (sec)  :  2.5E-05        T2 (sec)  :  2.1E-06        T3 (sec)  :  3.8E-11
f1  (Hz)  :  5.9E+03        f2  (Hz)  :  7.5E+04        f3  (Hz)  :  4.2E+09
R1 (Ohm)  :  1.3E+04        R3 (Ohm)  :  4.5E+02        R4 (Ohm)  :  3.8E+01
R2 (Ohm)  :  7.6E+03        C2 (Far)  :  5.6E-08        C3 (Far)  :  1.0E-12
C1 (Far)  :  1.0E-10

                    DYNAMIC PARAMETERS
Wn/2π                  (Hz)  :  1.0E+05  pull-in time          (sec)  :  5.4E-05
W_0dB/2π               (Hz)  :  1.7E+05  pull-in range         (Hz)  :  7.7E+05
zeta                         :  0.70     pull-out range       (Hz)  :  3.1E+05
overshoot               (%)  : 21.03     hold range           (Hz)  :  1.5E+06
Kv                           :  1.1E+07  settling time        (sec)  :  1.8E-06
Winput/W_0dB                 : 63.7      lock-in range        (Hz)  :  2.2E+05
phasemargin with C3  (deg)   :  67       ripple suppr. with C3 (dB) : -44
      without C3     (deg)   :  67                 without C3 (dB) : -44
W-3dB/2π closed loop (Hz)    :  2.0E+05
peak phase error     (deg)   :  4.3E-01
                                                    Philips Components
Optimize ? (Y/N): Y
```

(a)



(b)

Fig.66 (a)Loop parameters and (b) Bode plot of the FM demodulator after altering the pull-out range and removing C3.

FSK decoder

Using the PC3 phase comparator of the 4046A, it's straightforward to build a FSK (Frequency Shift Keying) decoder, see Fig.67(a). If the VCO is trimmed so that its centre frequency is exactly mid-way between the two frequency keys, in this example, at 1800 Hz, then an input signal of 1800 Hz will produce a phase difference of exactly 180°. With the VCO output frequency range set from 800 Hz to 2800 Hz, a signal of 1200 Hz causes the VCO to lower the average voltage of the comparator as shown in Fig.67(b), resulting in a logic LOW output of the HC/HCT74 D-flip-flop. The reverse happens if the input signal is raised to 2400 Hz, producing a logic HIGH.

For a fast settling time as required to receive data at high baud rates, the filter comprises only R3 and C2, because the calculated f_2 and f_3 were both far above the $\omega_{0\ dB}$ of the open loop and could thus be omitted. Figure 68 shows the results from the design program.

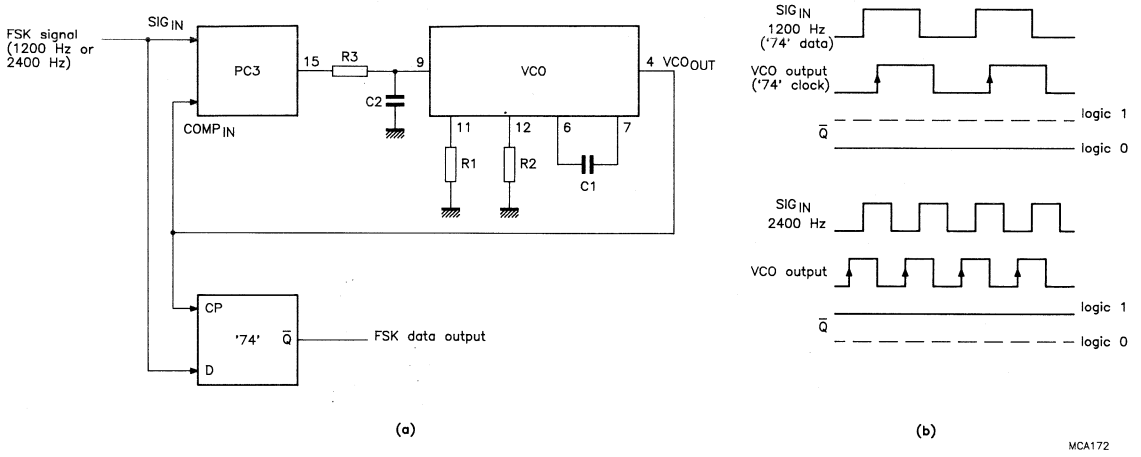
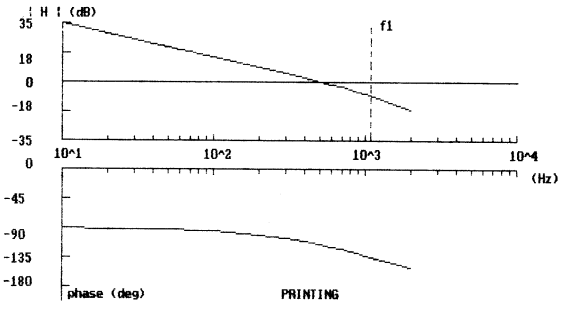


Fig.67 (a) FSK decoder using PC3 of the 4046A; (b) waveforms when the VCO centre frequency is set to 1800 Hz.

```
                        INPUT PARAMETERS
PC     :  3       fin  (Hz) :  1.800E+03    Spread input freq.  (%) :  0.0
N      :  1.0     2fR  (Hz) :  2.000E+03    Part-to-part spread (%) :  0.0
Filter :  1       f0   (Hz) :  1.800E+03    Vcc               (Volt) :  5.0

                     VCO and FILTER PARAMETERS
T1 (sec) :  6.6E-05          T2 (sec) :  8.6E-06       T3 (sec) :  8.6E-07
f1  (Hz) :  2.1E+03          f2  (Hz) :  1.9E+04       f3  (Hz) :  1.9E+05
R1 (Ohm) :  9.5E+04          R3 (Ohm) :  4.4E+02       R4 (Ohm) :  5.7E+01
R2 (Ohm) :  1.5E+06          C2 (Far) :  1.5E-07       C3 (Far) :  1.5E-08
C1 (Far) :  3.0E-08
                       DYNAMIC PARAMETERS
Wn/2π                (Hz) :  1.1E+03  pull-in time          (sec) :  1.2E-05
W_0dB/2π             (Hz) :  5.7E+02  pull-in range          (Hz) :  1.0E+03
zeta                      :  1.00     pull-out range         (Hz) :  1.0E+03
overshoot             (%) : 13.53     hold range             (Hz) :  1.0E+03
Kv                        :  3.6E+03  settling time         (sec) :  1.3E-04
Winput/W_0dB              :  3.2      lock-in range          (Hz) :  1.0E+03
phasemargin with C3 (deg) :  77       ripple suppr. with C3 (dB) :  -6
        without C3 (deg)  :  77                 without C3 (dB) :  -6
W-3dB/2π closed loop (Hz) :  2.7E+03
                                                      Philips Components
Optimize ? (Y/N): Y
```

(a)



(b)

Fig.68 (a) Results from the design program for the FSK decoder and (b) the Bode plot.

Crystal oscillator

A little known application for the 4046A is as a voltage-controlled crystal oscillator (VCXO), for example, when the part-to-part spread of the VCO is too large for the application but the input frequency is well-defined. Figure 69 shows the circuit.

The crystal is an 'AT'-cut oscillator crystal (such as Philips 4322 148 series in an RW-10 encapsulation, see Data Handbook C9, Piezoelectric quartz devices.) which operates near the anti-resonant or parallel mode. It may be necessary to fine-tune the crystal as indicated in Fig.69. The pulling characteristic of the crystal allows an operating temperature range from –40 °C to +85 °C, plus initial ageing accuracy tolerance factors, while still retaining lock between master and slave VCXOs.

For a 6 MHz crystal say with:

- a temperature stability of ±25 ppm from –40 °C to +85 °C
- calibration tolerance ±10 ppm
- long-term drift ±2 ppm,

the total (about ±37 ppm) means a capture and hold range of at least ±222 Hz over which two crystal-stabilized VCOs must track under worst-case conditions. Figure 70 shows the frequency stability of the VCXO as a function of ambient temperature. Table 4 lists some typical measured $2f_R$ for several crystals. The measurements were made without the trimmer capacitor C_T. In the case of the 6 MHz crystal, a ±222 Hz hold range is well within the $2f_R$ range of 1400 Hz specified in the example above. At frequencies below 3.1 MHz, the $2f_R$ becomes too small and the standard crystals will have too low a value for pullability (the listed value of 130 Hz is often already too small). At frequencies above 10 MHz, the VCO is unable to excite the crystal correctly and the VCO behaves as if the crystal was absent.

Table 4: Measured $2f_R$ for several VCXOs.

crystal freq. (Hz)	R2 (kΩ)	VCO output frequency (Hz) for an input voltage of:			$2f_R$ (Hz)
		1.1 V	2.5 V	3.9 V	
3 151 170	19.6	3 151 570	3 151 650	3 151 700	130
4 782 720	21.2	4 783 700	4 784 000	4 784 100	400
6 000 000	26.1	5 997 200	5 998 100	5 998 600	1400
8 867 238	26.1	8 843 400	8 858 900	8 862 400	19000
10 000 000	46.4	9 964 500	9 989 400	9 994 200	29700

V_{CC} = 5 V; T_{amb} = 25 °C; C_T = 0 pF.
The frequencies listed are for a typical set-up; actual values will differ slightly.

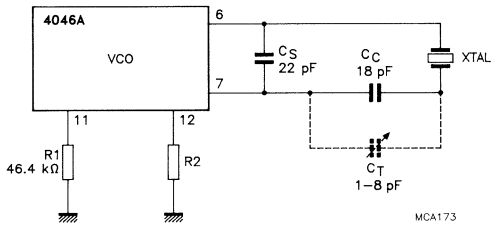


Fig.69 VCO connected as a VCXO.

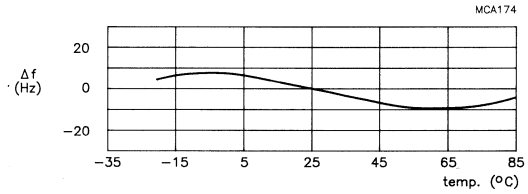


Fig.70 Frequency stability of the crystal.

Improving the settling time

When the settling time of a loop is too long for an application, and the requirements for ripple suppression don't allow any increase of loop bandwidth, the settling time can be reduced using the circuit shown in Fig.71. Note that this circuit can only be used with the PC2 comparator.

When a voltage step is applied to the input of the phase comparator, the average output voltage jumps away from the VCO input voltage. When R3'<< R3, say R3/10, initial tuning is via the diodes and R3', reducing the settling time. Once the original voltage difference has been reduced to less than one diode voltage drop, the loop returns to its original dynamic behaviour with better ripple suppression.

The dynamic behaviour (i.e. whether a loop is sufficiently damped) can be checked with the PLL design program. First, the total loop is designed with the desired ripple suppression ratio. Then the reduced value of R3 is inserted via option 10 of the optimization menu. Now, the new dynamic behaviour is calculated and a final check can be made using a Bode plot. If the results obtained are not optimum, the process can be repeated and the reduced value of R3 altered. The voltage drop across the diode can be modelled by increasing the VCO input voltage range by a factor $V_{CC}/(V_{CC}-V_{diode})$ which lowers the total gain of the loop.

Silicon or germanium diodes can be used depending on the expected input step and the gain of the VCO (set by $2f_R$).

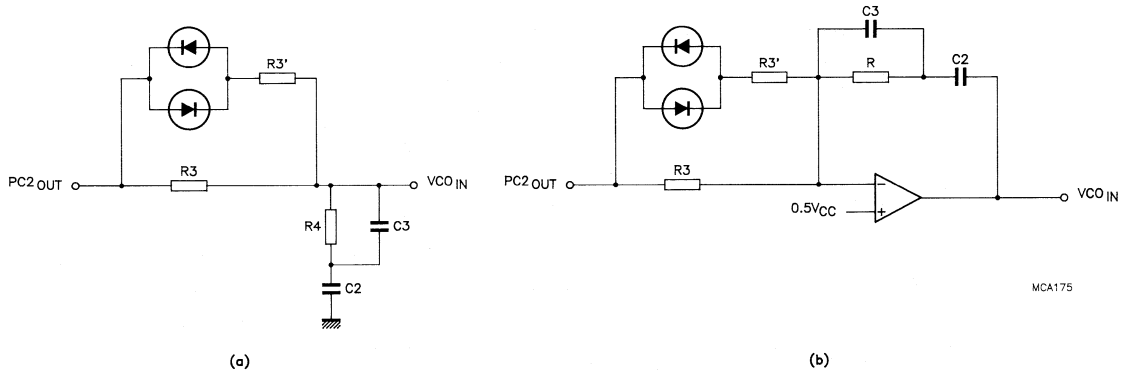


Fig.71 Circuit for reducing settling time (a) for a passive loop filter; (b) for an active loop filter.

APPENDIX A

Variable gain of PC2

When phase comparator PC2 is used with a passive low-pass filter, its gain (unlike that of PC1 and PC3) depends on the voltage on the filter capacitor. Let's consider PC1 with a passive filter first (Fig.A1), and calculate the transfer function and gain.

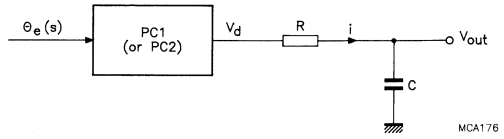


Fig.A1 Phase comparator (PC1 or PC2) with a passive filter.

To simplify matters, a simple RC filter is used, and from Fig.A1, the average output of PC1, $V_d(s)_{(avg)}$, is:

$$V_d(s)_{(avg)} = \frac{\theta_e(s)V_{CC}}{\pi} \tag{A1}$$

And:

$$V_{out}(s) = i/sC. \tag{A2}$$

In addition,

$$i = \frac{V_d(s) - V_{out}(s)}{R}$$

$$= \frac{\frac{\theta_e(s)}{\pi} \times V_{CC} - V_{out}(s)}{R} \tag{A3}$$

$V_{out}(s)$ can be eliminated in Eq.(A3), yielding:

$$V_{out}(s) = \frac{\theta_e(s)V_{CC}}{\pi sCR} \times \frac{s}{s + 1/RC} \tag{A4}$$

For a step input, $\theta_e(s) = \Delta\theta_e/s$, and Eq.(A4) becomes:

$$V_{out}(s) = \frac{V_{CC}}{\pi} \times \frac{\Delta\theta_e}{RC} \times \frac{1}{s(s + 1/RC)} \tag{A5}$$

Using the inverse Laplace transform, this is:

$$\frac{V_{out}(t)}{\Delta\theta_e} = \frac{V_{CC}(1 - e^{-t/RC})}{\pi} \tag{A6}$$

where V_{CC}/π is the phase comparator gain which is independent of the voltage on the capacitor.

Now consider the situation with PC2, see Fig.A1 again. If PC2 starts from a 3-state condition, the initial capacitor voltage must be included in the calculations, so now:

$$V_{d(avg)} = V_{out}(s) + \{V_{CC}/s - V_{out}(s)\}\Delta\theta_e/2\pi \tag{A7}$$

assuming $\Delta\theta_e > 0$.

And:

$$V_{out}(s) = V_{C0}/s + i/sC \tag{A8}$$

where V_{C0} is the initial voltage on the capacitor C.

In addition,

$$i = \{V_d(s) - V_{out}(s)\}/R$$

$$= \{V_{CC}/s - V_{out}(s)\Delta\theta_e/2\pi\} \tag{A9}$$

From Eqs. (A8) and (A9),

$$V_{out}(s) = \{V_{C0}/s + \{(V_{CC}/s - V_{out}(s))\}\Delta\theta_e/2\pi \quad (A10)$$

which can be rewritten as:

$$V_{out}(s) = [s\tau/(1 + s\tau)] \times (V_{C0}/s + V_{CC}/s^2\tau) \quad (A11)$$

$$= \frac{V_{C0}}{(s + 1/\tau)} + \frac{V_{CC}}{s\tau(s + 1/\tau)} \quad (A12)$$

where $\tau = 2\pi RC/\Delta\theta_e$.

Using the inverse Laplace transform, this is:

$$V_{out}(t) = V_{CC} - (V_{CC} - V_{C0})\exp(\Delta\theta_e t/2\pi RC) \quad (A13)$$

Using the series expansion for exp x, and neglecting terms $x^2/2!$ and higher (true for $\Delta\theta_e << 2\pi$), Eq.(A13) can be rewritten as:

$$V_{out}(t) = V_{C0} + (V_{CC} - V_{C0})\Delta\theta_e t/2\pi RC \quad (A14)$$

For small values of $\Delta\theta_e$,

$$\frac{V_{out}(t)}{\Delta\theta_e} = (V_{CC} - V_{C0})/2\pi \times t/RC \quad (A15)$$

gain of PC2 | transfer characteristic of filter (integrator)

If V_{C0} = 2.5 V, the average value of the gain is $V_{CC}/4\pi$ (the value stated in the data sheet). At V_{CC} = 5 V, and using the VCO input voltage range as the limit for V_{C0}, the gain of PC2 can vary from $1.1/2\pi$ to $3.9/2\pi$. So, for a synthesizer, for example, built using PC2 and a passive filter, the gain will vary over this range as the division ratio is altered from N_{min} to N_{max} since this will alter the VCO input voltage from minimum to maximum.

In the PLL design program, this gain variation is taken into account, when the division ratio is changed (option 0 of the optimize menu). However, an unwanted gain difference still exists for positive or negative phase errors when $V_{C0} \neq 0.5V_{CC}$.

If it is anticipated that the full VCO input voltage range will be used (e.g. in synthesizer applications), it is recommeded to use an active filter, see Fig.A2, which keeps V_{C0} constant, resulting in a constant PC2 gain even for large phase errors. In Fig.A2,

$$i = (V_{CC} - 0.5V_{CC}) \times \frac{\theta_e(s)}{2\pi} \times \frac{1}{R} \quad (A16)$$

and

$$V_{out}(s) = -i/sC$$

$$= \theta_e(s)\{-V_{CC}/4\pi RCs\} \quad (A17)$$

For a step, $\theta_e(s) = \Delta\theta_e/s$, and Eq.(A17) becomes:

$$V_{out}(s) = -\Delta\theta_e V_{CC}/4\pi RCs^2 \quad (A18)$$

Using the inverse Laplace transform, this is:

$$\frac{V_{out}(t)}{\Delta\theta_e} = -V_{CC}/4\pi \times t/RC \quad (A19)$$

gain of PC2 | transfer characteristic of filter (integrator)

Note that when PC2 is used, a passive filter and an active filter have the same ideal integrator characteristic, see Eqs.(A15) and A(19). This means that even when a passive filter is used with PC2, the loop behaves as though an active filter is present. However, the gain of PC2 when used with a passive filter will vary, as described earlier.

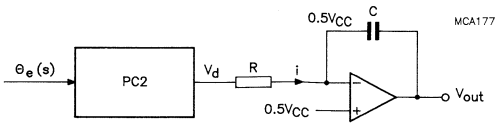


Fig.A2 PC2 with an active filter.

APPENDIX B

Transient response calculations

Figure B1 shows a general feedback system. The transfer function is:

$$H(s) = \frac{A(s)}{1 + A(s)B(s)} \quad \text{(B1)}$$

The error function is:

$$H_e(s) = \theta_e(s)/\theta_i(s)$$

$$= \frac{1}{1 + A(s)B(s)}$$

$$= 1 - H(s) \quad \text{(B2)}$$

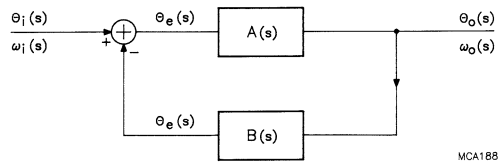


Fig.B1 Basic feedback system.
$\omega_e(s) = \omega_{out}(s) - \omega_{in}(s)$
$A(s) = (K_o/s)K_dF(s)$
$B(s) = 1/N$ (divider)
$F(s)$ = filter transfer function
K_o = VCO gain
K_d = phase comparator gain.

Table B1 lists the transient response when the input is excited by a phase step, a frequency step or a frequency ramp.

Table B1: Transient response definitions

	phase step $\theta_i(s) = \Delta\theta_i/s$	frequency step $\omega_i(s) = \Delta\omega_i/s$	frequency ramp $\omega_i(s) = \Delta\omega_i/s^2$
phase response: $\theta_2(s)$	$\frac{\Delta\theta_i H(s)}{s}$	$\theta_i(s)H(s) = \frac{\Delta\omega_i H(s)}{s^2}$	$\frac{\Delta\omega_i H(s)}{s^3}$
phase error: $\theta_e(s)$	$\frac{\Delta\theta_i H_e(s)}{s}$	$\frac{\Delta\omega_i H_e(s)}{s^2}$	$\frac{\Delta\omega_i H_e(s)}{s^3}$
frequency response: $\omega_0(s)$	$s\theta_2(s)=\Delta\theta_i H(s)$	$\frac{\Delta\omega_i H(s)}{s}$	$\frac{\Delta\omega_i H(s)}{s^2}$
frequency error: $\omega_e(s)$	–	$\frac{\Delta\omega_i H_e(s)}{s}$	$\frac{\Delta\omega_i H_e(s)}{s^2}$

Active filter

First, the transient response of a PLL using an active filter is calculated. In this case,

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{(B3)}$$

$$H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{(B4)}$$

The phase response to a phase step is:

$$\theta_2(s) = \frac{\Delta\theta_i}{s} \times H(s)$$

$$= \frac{\Delta\theta_i}{s} \times \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{B5}$$

Using the inverse Laplace transform and φ = arc sinζ yields:

$$\theta_2(t) = \Delta\omega_i(t)\{1 - \frac{1}{\sqrt{(1-\zeta^2)}} \times \cos[\sqrt{(1-\zeta^2)}\omega_n t + \varphi]e^{-\zeta\omega_n t}\} \tag{B6}$$

and the phase error is:

$$\theta_e(t) = \theta_i(t) - \theta_2(t) = \Delta\theta_i(t)\frac{1}{\sqrt{(1-\zeta^2)}} \cos\{[\sqrt{(1-\zeta^2)}\omega_n t + \varphi]e-\zeta\omega_n t\} \tag{B7}$$

Equation (B7) describes the curves of Fig.41, which could have been expected because the phase response to a phase step is the same as the frequency response to a frequency step. This can be verified in Table B1, bearing in mind that $\theta = \omega/s$.

The phase response to a frequency step (which is the same as the frequency response to a frequency ramp) can be calculated in a similar way.

$$\theta_2(s) = \frac{\Delta\omega_i}{s^2} \times H(s) = \Delta w_i \times \left\{ \frac{1}{s^2} - \frac{1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right\} \tag{B8}$$

Using the inverse Laplace transform yields:

$$\theta_2(t) = \Delta\omega_i\{t - \frac{e^{-\zeta\omega_n t} \sin\sqrt{(1-\zeta^2)}\omega_n t\}}{\omega_n\sqrt{(1-\zeta^2)}} \tag{B9}$$

And the phase error (with $\theta_i(t) = \Delta\omega_i t$) is:

$$\theta_e(t) = \theta_i(t) - \theta_2(t) = \frac{\Delta\omega_i e^{-\zeta\omega_n t} \sin\sqrt{(1-\zeta^2)}\omega_n t}{\omega_n\sqrt{(1-\zeta^2)}} \tag{B10}$$

This function describes the curves of Fig.42.

The phase error due to a frequency ramp is determined as follows.

$$\theta_e(s) = \frac{\Delta\omega_i^3}{s^3} \times H_e(s)$$

$$= \frac{\Delta\omega_i}{s^3} \times \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{B11}$$

$$= \frac{\Delta\omega_i}{\omega_n^2} \times \left\{ \frac{1}{s} - \frac{s + \omega_n\zeta + \omega_n\zeta}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right\} \tag{B12}$$

Using the inverse Laplace transform yields:

$$\theta_e(t) = \frac{\Delta\omega_i}{\omega_n^2} \times \{1 - e^{-\zeta\omega_n t} [\cos\sqrt{(1-\zeta^2)}\omega_n t + \frac{\zeta\sin\sqrt{(1-\zeta^2)}\omega_n t]\}}{\sqrt{(1-\zeta^2)}} \tag{B13}$$

With φ = arc sin ζ:

$$\theta_e(t) = \frac{\Delta\omega_i}{\omega_n^2} \times \left\{ \frac{[1 - e^{-\zeta\omega_n t}] \cos [\sqrt{(1-\zeta^2)}\omega_n t - \varphi]}{\sqrt{(1-\zeta^2)}} \right\} \tag{B14}$$

This function describes the curves of Fig.40.

Passive filter

For a passive filter, the transfer function is:

$$H(s) = \frac{\omega_n^2(s\tau_2 + 1)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \text{(B15)}$$

with τ_1 = R3C (C is the filter capacitor)

τ_2 = R4C.

The phase response to a phase step (or the frequency response to a frequency step) is:

$$\theta_2(s) = \Delta\theta_i \times \left\{ \frac{1}{s} - \frac{s + 2\zeta\omega_n - \omega_n^2\tau_2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right\} \qquad \text{(B16)}$$

Using the inverse Laplace transform yields:

$$\theta_2(t) = \Delta\theta_i \left\{ 1 - e^{-\zeta\omega_n t}\left[\cos\sqrt{(1-\zeta^2)}\omega_n t + \frac{\zeta\sin\sqrt{(1-\zeta^2)}\omega_n t}{\sqrt{(1-\zeta^2)}} - \frac{\omega_n\tau_2\sin\sqrt{(1-\zeta^2)}\omega_n t}{\sqrt{(1-\zeta^2)}}\right] \right\} \qquad \text{(B17)}$$

And the phase error is:

$$\theta_e(t) = \Delta\theta_i \frac{e^{-\zeta\omega_n t}}{\sqrt{(1-\zeta^2)}} \{\cos[\sqrt{(1-\zeta^2)}\omega_n t - \varphi] - \omega_n\tau_2\sin[\sqrt{(1-\zeta^2)}\omega_n t]\} \qquad \text{(B18)}$$

With $\tau_2 = 0$, this is the function of Fig.40.

Another approach is to substitute $2\zeta\omega_n - \omega_n^2\tau_2 = 1/(\tau_1 + \tau_2)$ in Eq.(B16), and transforming to the time domain yields:

$$\theta_2(t) = \Delta\theta_i \left\{ 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{(1-\zeta^2)}} [\cos\sqrt{(1-\zeta^2)}\omega_n t + \varphi] + \omega_n/K_d K_o \sin[\sqrt{(1-\zeta^2)}\omega_n t] \right\} \qquad \text{(B19)}$$

and the phase error is:

$$\theta_e(t) = \Delta\theta_i \frac{e^{-\zeta\omega_n t}}{\sqrt{(1-\zeta^2)}} \{\cos[\sqrt{(1-\zeta^2)}\omega_n t + \varphi] + \omega_n/K_d K_o \sin[\sqrt{(1-\zeta^2)}\omega_n t]\} \qquad \text{(B20)}$$

For a high-gain loop, $K_d K_o >> \omega_n$, and Eq.(B21) describes Fig.41. Depending on the gain of the loop and the passive filter used, there is a gradual change from Fig.40 to Fig.41. When PC2 is used, the gain is extremely high and Fig.41 is always valid.

APPENDIX C

Bode plot measuring circuit

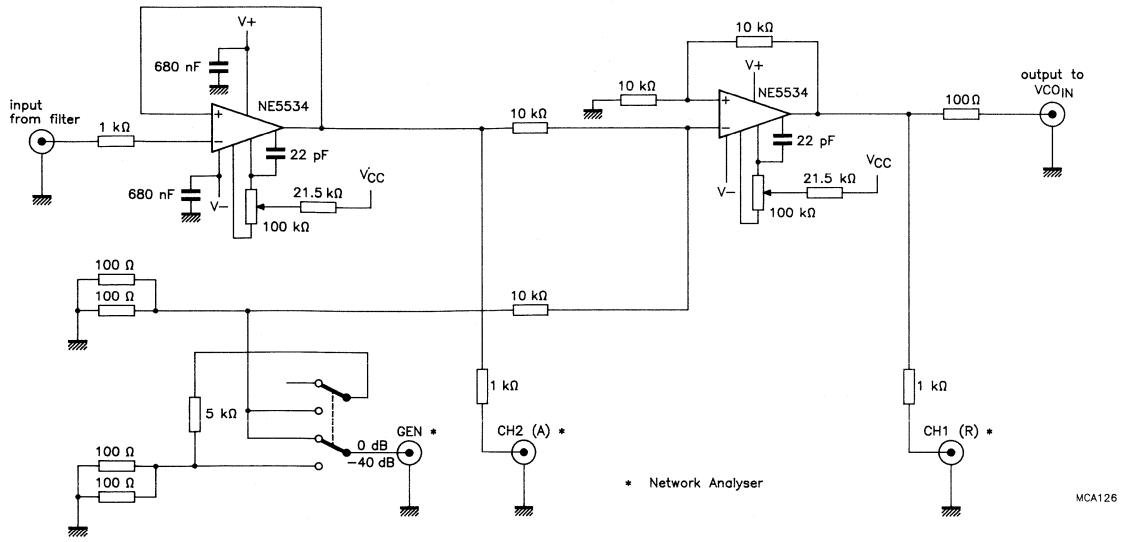


Fig.C1 Bode plot measuring circuit. This circuit was used with a Hewlett Packard network analyser type 3577A.

APPENDIX D

Symbols

$\pm\Delta\omega_H$	hold range (see Fig.2)
$\pm\Delta\omega_{LH}$	lock-in range (see Fig.2)
$\pm\Delta\omega_{PI}$	pull-in range (see Fig.2)
$\pm\Delta\omega_{PO}$	pull-out range (see Fig.2)
$2f_R$	VCO output frequency range (see Fig.2)
B_i	noise bandwidth of the input signal
B_L	noise bandwidth of a loop
f_0	VCO centre frequency
f_{min}	the minimum frequency of the VCO
f_{max}	the maximum frequency of the VCO
f_{off}	VCO offset frequency
f_{in}, ω_{in}	frequency of the input signal
ϕ_{in}	phase of the input signal
f_{out},ω_{out}	frequency of the output signal
ϕ_{out}	phase of the output signal
H(s)	closed-loop transfer function
$H_e(s)$	closed-loop error function
K_d	phase comparator conversion gain
K_o	VCO conversion gain
K_v	total loop conversion gain (K_oK_d/N)
N	division ratio of a ÷N counter
s	Laplace operator
T_{AV}	average time before losing lock due to phase noise
T_p	pull-in time
T_S	settling time
$T_{S(5\%)}$	settling time (output within 5% of the applied step)
ω_n	natural frequency
ω_{3dB}	the 3 dB bandwidth of the closed-loop gain
ζ	damping factor

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